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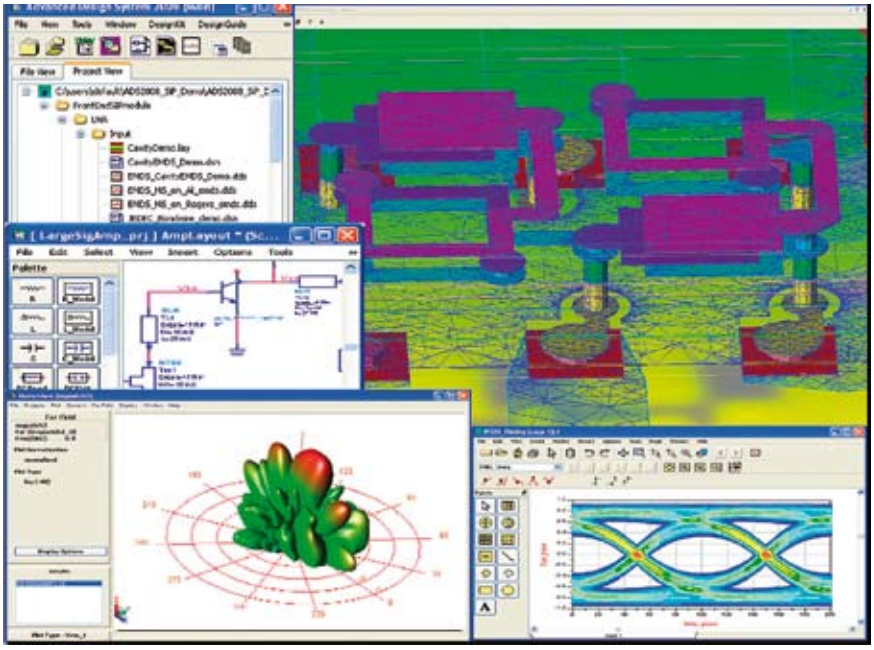
Agilent Technologies announces Integrated, 3D EM Simulation Solution for RF Module Design

EMDS-for-ADS eliminates need for standalone EM tools, improves productivity

Agilent Technologies

EMDS-for-ADS helps designers accurately predict the 3D EM interactions of embedded passive components in RF modules while co-simulating with active circuits to maximize the wireless sub-system performance. The integrated 3D EM simulator improvements allow designers to analyze larger circuits faster without leaving their familiar design flow. This capability increases productivity in the overall design and verification process.

"The 3D EM simulator allows our RF module designers to replace standalone tools such as HFSS," said Bob Wong, R&D engineer with Agilent's Component



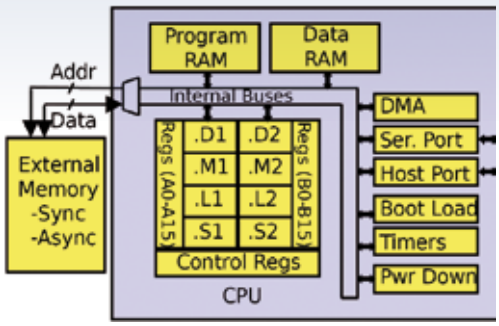
The integrated 3D electromagnetic analysis capabilities in Advanced Design System 2008, Update 2, eliminate the need for standalone EM tools and improve productivity

FlexWare project invites you to an open user group meeting on December 16th

FlexWare

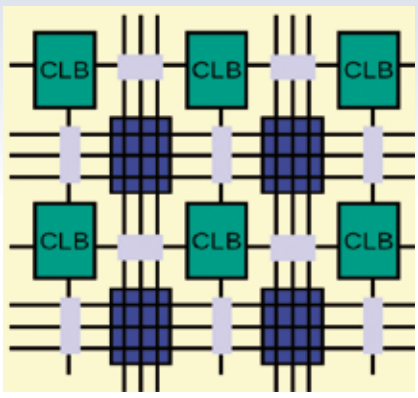
The FlexWare project targets the efficient design of hardware accelerators for algorithms with massive, low-level parallelism, organized in regular loop structures.

Applications from various domains fit this description, e.g., video and image processing, finite element simulation, medical imaging, speech processing, bioinformatics applications, ...



DSP

To realize cost-effective accelerators, we propose to use flexible, parallel hardware platforms. These platforms are retargetable, either by platform reconfiguration or by executable code generation, and offer sufficient low-level data path and memory parallelism. Today, a range of hardware platforms with different types and degrees of parallelism exist or are being developed. When faced with a new application, it is far from obvious which platform would offer the best cost-performance. To drastically reduce the R&D cost of accelerating new algorithms, this project targets at developing new methods and tools for guiding the discrimination between alternative platforms, as well as for automatically extracting application parallelism and optimally mapping it to the resources offered by several specific hardware platforms.



FPGA

Test (Network Analyzer) Division. *"As a result, we've more than doubled our design efficiency because we can interactively co-simulate the circuit and physical 3D effects without leaving the ADS design flow."*

EMDS-for-ADS accounts for the finite dielectric boundaries of RF modules. In addition, it is useful for verifying the accuracy of faster Planar EM simulators such as Agilent's Momentum, which assumes infinite dielectric planar layers in its analysis. EMDS-for-ADS also features a new finite element mesher and high-capacity iterative solver that delivers better accuracy, speed and capacity for RF SIP (system-in-package) and RF module designs.

The most common applications for EMDS-for-ADS are RF modules based on LTCC (low temperature co-fired ceramics) and laminates with embedded passive structures. They are found in almost all RF modules produced today. EMDS-for-ADS saves time when drawing these structures with its planar RF layout macros. These macros automatically draw RF components such as spiral inductors and meander lines – which are time-consuming to construct using a generic 3D drawing and simulation tool.

EMDS-for-ADS is part of the new Agilent Advanced Design System 2008 Update 2. Advanced Design System is a powerful electronic design automation platform, offering complete integration to designers of consumer and commercial wireless electronic products such as mobile phones, wireless networking and GPS, as well as radar and satellite communications systems, and high-speed digital serial links.

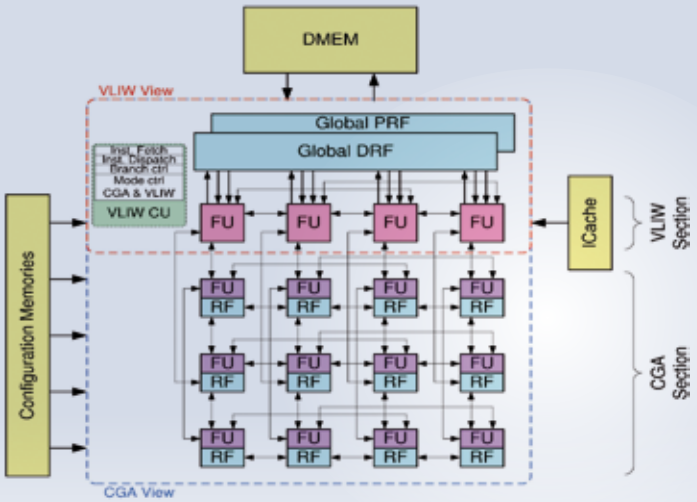
About Agilent EEsof EDA Software

Agilent EEsof EDA is an industry-leading provider of RF-mixed signal circuit and system-design software. Agilent EEsof EDA software is compatible with and is used to design the company's test and measurement equipment. Additional information is available at www.agilent.com/find/eesof.

More information about ADS 2008 Update 2 is available at www.agilent.com/find/eesof-ads2008-update2-pr. To request a demo of ADS 2008 Update 2, visit www.agilent.com/find/eesof-ads2008-update2-demo-pr. ■

About Agilent Technologies

Agilent Technologies Inc. (NYSE: A) is the world's premier measurement company and a technology leader in communications, electronics, life sciences and chemical analysis. The company's 20,000 employees serve customers in more than 110 countries. Agilent had net revenues of $5.4 billion in fiscal 2007.



ADRES

We focus on four flexible, parallel computing platforms: FPGA, ADRES, FEENECS and DSP.
Together, they cover a range of degrees of flexibility and different types of parallelism. FPGAs are fully reconfigurable, offering maximal flexibility, ample distributed memory bandwidth and data path parallelism at the cost of clock speed. DSPs are tailored for signal processing, offer limited parallelism, but operate at high clock rates. Somewhere between those two are the flexible parameterized architectures, ADRES and FEENECS that have been recently developed at IMEC. ADRES combines a very long instruction word (VLIW) processor, efficient for executing control-flow code, with a coarse-grain reconfigurable processing array that accelerates loops by exploiting high degrees of loop-level parallelism. FEENECS is a VLIW processor with extremely long instruction words. It contains very wide registers that are tightly coupled with large scratch pad memories and a massively parallel data path.

To achieve a first understanding of the relative strengths and weaknesses of the different types of hardware platforms, a bioinformatics application, the Smith-Waterman sequence alignment, has been implemented on the four platforms.
Since this algorithm is perfectly fit for an implementation on a systolic array, the FPGA implementation reaches the highest performance but also has the highest development cost. FEENECS and ADRES result in a high energy efficiency, while the DSP implementation has the lowest engineering cost.

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IMEC has developed an innovative architecture for flexible FEC (Forward Error Correction). The solution targets data transmission applications that need to combine flexibility, high throughput, and low power consumption. Examples are future wireless terminals and optical storage. IMEC's FEC enables, on one processor, the turbo- and LDPC decoding of major communication standards. The technology is available for the industry either through a soft IP transfer, or through joint R&D projects.

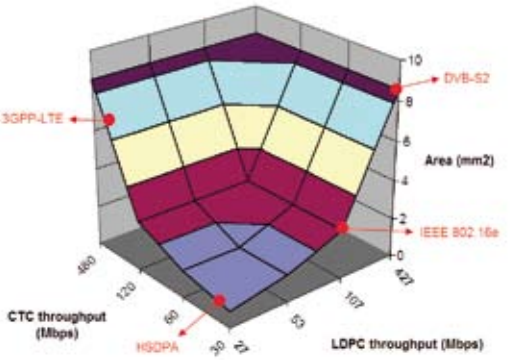
IMEC announces scalable architecture for flexible FEC

IMEC's FEC solution supports both turbo- and LDPC coding, including multi-channel operation over different modes. It is the world's first ASIP (application-specific integrated processor) for flexible FEC enabling both turbo- and LDPC coding for 3rd generation mobile phones (3GPP-LTE), wireless networks (IEEE802.11n, IEEE802.16(e)) and television broadcasting (DVB-S2/T2, GB20600). Support for other convolutional turbo-code or LDPC codes can be enabled through assembly programming. A combined multiprocessor and ultra-wide SIMD (Single Instruction, Multiple Data) approach achieves scalability, high throughput and high energy efficiency.

The preliminary estimates for throughput and energy consumption show that IMEC's FEC solution is competitive with solutions that separate turbo and LDPC decoding on dedicated hardware. The throughput that is achieved is between 0.07 to 1.25Mbps/MHz, with efficiencies from 0.3 to 0.5nJ/bit/iter in turbo mode and 0.08 to 0.1nJ/bit/iter in LDPC mode. The silicon area used by the flexible solution is comparable to the sum of multiple dedicated solutions.

The new flexible FEC fits in IMEC's research strategy to design flexible components for data transmission. These are targeted at, amongst others, future mobile terminals; they combine high throughput, low power consumption, and a small footprint. Other IMEC components that follow this vision are a flexible RF transceiver and a flexible baseband chip. IMEC invites partners to collaborate in this research through its joint research programs. Industrial players can also profit from IMEC's research by licensing the components.

FEC is used in all digital transmitters and receivers to ensure that the digital message is sent free of errors. When the transmitter sends a message, it encodes the bit stream, adding redundant data. These allow the receiver to detect and correct errors - within some bounds - without asking the transmitter for additional data. State-of-the-art FEC mainly uses 2 methods of FEC coding: turbo codes and LDPC codes. These are popular because they allow high-speed FEC encoding and decoding. But turbo codes and LDPC codes are complex, and decoding them puts a heavy computational load on the receiver. Therefore, until recently, FEC decoders for the different FEC methods were implemented as dedicated hardware blocks, focusing on minimum power consumption and area, and thereby sacrificing flexibility.■



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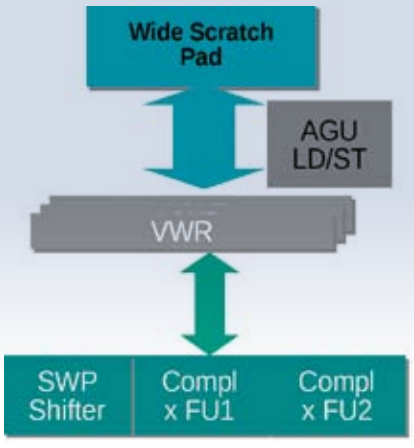

VLIW

FlexWare project invites you to an open user group meeting on December 16th

Since the Smith-Waterman algorithm is not representative for all potential target applications we are seeking for new potential applications, both within and outside the bioinformatics domain.
They will be used to test the compilers and design tools that are developed within the project, and further investigate which kinds of platforms best fit which kinds of applications.

We invite companies to become a member of our user group. There will be an open user group meeting on December 16th (at 2 pm in "het Pand", Gent, Belgium). At this event we will give an overview of the project, present current results and plans for the future. All interested companies are welcome.
More information can be found on our website: http://flexware.elis.UGent.be ■

How to develop a coding standard for an embedded project?

http://www.dspvalley.com

High Tech Campus, Eindhoven
December 3, 2008

On December 3rd, 2008 DSP Valley will organize a seminar about coding standards for embedded software development.
The use of coding standards for programming embedded systems has been growing recently because they reduce the risk of expensive and embarrassing coding flaws slipping into production devices. There are several popular standards like MISRA-C, JSF and JPL in use today, but each has been designed for use in different situations and there is surprisingly little overlap between the rules.
During this seminar experts from industry will share with you their experiences and best practices. An overview of some of the tools that can help you to follow these rules will also be presented.
The seminar is meant for embedded software engineers, system engineers and project managers who are interested in developing 'high quality' software.
In parallel to the presentations a mini-exhibition will show products and demos.
We will provide time and opportunity to network with the different participants and presenters to allow discussions on details.

The complete program details will be available on our website: http://www.dspvalley.com

All the presentations will be given in English.

For more information please contact Filiep Vincent (filiep.vincent@dspvalley.com or +32 16 24 14 43)

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Working with Jos was a clear win-win situation: the success of DSP Valley on the one hand contributed to the success of the R&D activities of Philips and NXP in Leuven and their continuous growth on the other hand, and vice-versa.

Now, after more than 10 years of fruitful cooperation, mutual thrust and personal mentorship and friendship, Jos has decided to retire and to enjoy his life with his wife and family and to spend time to his passion of playing the piano.

Jos, on behalf of the board of DSP Valley, all DSP Valley members from industry and academia, we thank you for all the years of your unconditional support to the cluster of the DSP community in and around Leuven, and we wish you all the best!

Thank you! ■

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Agilent Technologies announces Integrated, 3D EM Simulation Solution for RF Module Design • p.1
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IMEC announces scalable architecture for flexible FEC • p.4
IMEC integrates SDR-enabling technology • p.7
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AnSem expands its operations with the opening of a new design center in Bucharest, Romania • p.5
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Barco and Ingenient Technologies announce business partnership toward European customers • p.6
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Sensata Technologies adopts Target's IP Designer for use in next-generation automotive products • p.8
ETRI selects Target as its ASIP tools Provider for the Design of Next-Generation Multi-Core Media Processors • p.8
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