A Coarse-Grained Array Accelerator for Software-Defined Radio Baseband Processing

A shrinking energy budget for mobile devices and increasingly complex communication standards make architecture development for software-defined radio very challenging. Coarse-grained array accelerators are strong candidates for achieving both high performance and low power. The C-programmable hybrid CGA-SIMD accelerator presented here targets emerging broadband cellular and wireless LAN standards, achieving up to 100-Mbps throughput with an average power consumption of 220 mW.

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Wireless technology is considered a key enabler of future consumer products and services. To cover the extensive range of applications, future handheld devices must support a wide variety of wireless communication standards concurrently. The growing number of air interfaces makes traditional implementations based on the integration of multiple specific radios and baseband ICs cost-ineffective. By contrast, software-defined radios (SDRs) achieve flexibility and cost-efficiency by deploying baseband processing on programmable or reconfigurable processors.[1] Researchers in academia and industry have already proposed several SDR platforms, of which most support current wireless standards such as W-CDMA (UMTS)—Wideband Code Division Multiple Access (Universal Mobile Telecommunications System)—IEEE 802.11 b/g, and IEEE 802.16.[1–5]

However, a major challenge remains in implementing emerging multicarrier and multi-antenna standards while maintaining cost-effectiveness: Compared to the current wireless standards, standards such as IEEE 802.11 n and LTE (Long Term Evolution) represent a tenfold increase in complexity and in required throughput. Technology scaling will no longer suffice to sustain the complexity increase. Instead, we must revise architectures to achieve the required performance at energy budgets that are acceptable for handheld integration (about 300 mW). This revision must take into account the key characteristics of wireless baseband processing: Most of the computation time is spent in inner loops (also known as kernels) that feature high data-level parallelism (DLP) and high instruction-level parallelism (ILP), corresponding to simple control flow.

This article presents the design, implementation, and performance evaluation of a C-programmable hybrid coarse-grained array, single-instruction, multiple-data (CGA-

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