The Energy Scalability of Wavelet-based, Scalable Video Decoding

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Abstract. Scalable video allows to decode a single video stream, or part of it, at varying quality of service (QoS). Since the amount of calculations scales with the QoS, energy dissipation is expected to scale similarly. To investigate the relation between QoS and energy dissipation we actually measured the energy dissipation of a scalable video decoder implementation on an FPGA. The measurements show how dissipation effectively scales with QoS and indicate how energy can be saved by rescaling the QoS and reconfiguring the FPGA accordingly.

1 Introduction

Scalable video is a hot topic in the multimedia community. "Scalable" means that the quality of service (QoS), i.e. the image quality, frame rate, resolution and color depth of the decoded video, can be freely adapted without having to re-encode the video stream or having to decode the whole video stream if only a lower quality version is required. Scalable video has advantages for both the server (the provider of the content) and the clients. On the one hand, the server scales well since it has to produce only one encoded video stream that can be broadcast to all clients, irrespective of their QoS requirements. On the other hand, the client (or the network) can easily adapt the decoding parameters to its needs. This way it is possible to optimize the use of the network, the display, the required processing power, the required memory, ...

Scalable video decoders have a very high complexity. Therefore, a real-time implementation of a scalable video decoder requires the use of specialised hardware that can provide sufficient computational power. Field Programmable Gate Arrays (FPGA) [2] are a perfect fit to decode scalable video because they can provide the required computational power. Moreover, they offer flexibility because they can be reconfigured each time the QoS requirements change. In the RESUME project[1], we explored hardware accelerated scalable video by actually developing an FPGA implementation of a wavelet based scalable video decoder. The real power of implementing a scalable video decoder in reconfigurable hardware is in the fact that different QoS requirements can be handled by different hardware instantiations so that the hardware resources are truly scaled together with the scaling of the QoS.

In this paper we study the relation between the energy dissipated by the decoder hardware and the delivered QoS. Our FPGA design was not optimized primarily for

[1] http://www.elis.ugent.be/resume