FPGA design Methodology for a Wavelet-Based Scalable Video Decoder

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Abstract. Client-side diversification led the video-coding community to develop scalable video-codecs supporting efficient decoding at varying quality levels. This scalability has a lot of advantages but the corresponding decoding algorithm is complex and really stresses the system bandwidth as it replaces the block-based DCT-approach with frame-based wavelets. This has a tremendous impact on the hardware architecture. We present the implementation of the RESUME decoder using reconfigurable hardware designed through the use of state-of-the-art HW/SW-codesign techniques. These techniques were augmented with automatic loop transformations and regression testing. Our efforts resulted in a design capable of decoding more than 25 frames per second at lossless CIF resolution.

1 Introduction

The RESUME[1] project [1] explores the benefits of using reconfigurable hardware for the implementation of scalable multimedia applications by building an FPGA implementation of a scalable, wavelet-based video decoder. The term 'scalable video' refers to a coding scheme that can easily accommodate changes in a QoS-level (Quality Of Service) with minimal computational overhead. A scalable video stream can be decoded at varying frame rates, resolutions and image quality by skipping redundant parts in the video stream, only decoding those parts that will contribute to the displayed video.

In SAMOS-IV [10] we explored the performance and resource requirements of RESUME's scalable wavelet-based video decoder through analytical means. We predicted that modern FPGAs would offer enough computational power but managing the memory bandwidth would be really challenging. In this paper we present the applied design methodology and the actual implementation results.

In the remainder of this paper we present an overview of the scalable video coding algorithm and the system specification for the decoder in Section 2. We elaborate on our design methodology, architecture, software and decisions in Section 3. We emphasize the importance of testing in Section 4 and illustrate the magnitude and complexity of our design by enumerating the applied design automation tools in Section 5. Section 6 summarizes the implementation results and Section **??** details about future work. Finally, in Section 7 we conclude this paper.

[1] Reconfigurable Embedded Systems for Use in Scalable Multimedia Environments