Nyquist-criterion based design of a CT $\Sigma\Delta$-ADC with a reduced number of comparators

J. De Maeyer, P. Rombouts and L. Weyten
Ghent University, Electronics and Information Systems (ELIS),
St.-Pietersnieuwstr. 41, 9000 Ghent, Belgium
jpdmaeye,rombouts,weyten@elis.ugent.be

***Abstract*— In this paper we present the design of a continuous time $\Sigma\Delta$-modulator in a 0.35 μm technology. While using a 6-bit internal quantizer a total of only 15 comparators were implemented. The inherent loop delay is accounted for in the design by using a design strategy based on the Nyquist stability criterion and the vector gain margin. Measurement results show a Peak SNR of 82 dB and a dynamic range of 85 dB for a bandwidth of 1.5 MHz.**

I. Introduction

Continuous time $\Sigma\Delta$-modulators with a NRZ-pulse are known to have some major advantages over their discrete time counterparts. However, one of the disadvantages is their sensitivity to clock jitter. Several pulses like the SCR-pulse or the sinusoidal pulse have been presented to decrease this sensitivity. However, the SCR-pulse increases the slew-rate requirements on the analog parts and the sinusoidal pulse is difficult to implement. Another way out would be to decrease the quantization step (Δ), since the jitter error is proportional to Δ. However, to the authors' knowledge the resolution of the internal quantizer in a continuous time $\Sigma\Delta$-modulator was limited to 4 or 5 bit, e.g. [1]. In this paper the design of a modulator with a quantizer having a quantization step corresponding to a 6-bit internal quantizer is presented. The capacitive load of the quantizer is kept limited through the use of the technique presented in [2]. For the design of the third order loop filter a Nyquist-criterion based design approach was used [3].

II. Architecture

In a conventional $\Sigma\Delta$-modulator [4], [5] the signal at the input of the internal quantizer ($V_{R,conv}$) is given by:

$$V_{R,conv}(z) = [STF(s)V_{in}(s)]^* + NTF(z)Q(z) \qquad (1)$$

Here, NTF denotes the noise transfer function while STF stands for the signal transfer function as defined in [6]. Concentrating on this first term, the input signal $V_{in}(s)$ is propagated through the STF after which it is sampled. This sampling operation is indicated in short by the *-operator [6]. If the maximum signal level of $V_{R,conv}(z)$ exceeds the full range input V_{FS} of the quantizer the quantizer becomes overloaded and the modulator (probably) unstable. Since, the STF equals one for the frequency range of interest, the full scale of the quantizer is chosen identical to that of the modulator. In such a conventional modulator the relationship between V_{FS} and Δ in the case of an L-bit quantizer equals:

$$\#comparators = \frac{V_{FS}}{\Delta} = 2^L - 1 \qquad (2)$$

Hence, each reduction of Δ with a factor of two results in a doubling of the number of comparators. In our case of a 6-bit quantizer 63 comparators are required.

In the designed modulator the number of comparators was greatly reduced. This was achieved by the use of the architecture of Fig. 1. In this architecture the input-output behavior of the dashed rectangular is identical to that of a normal quantizer. As such this architecture collapses to that of a conventional modulator [2]. E.g. one can show that the output of the modulator equals:

$$\begin{aligned} D(z) = &([V_{Q1}(s)]^* - V_{Q2}(z))\, NTF(z) \\ &+ Q(z)NTF(z) + [STF(s)V_{in}(s)]^* \end{aligned} \qquad (3)$$

In the architecture of Fig. 1 the signals $[V_{Q1}(s)]^*$ and $V_{Q2}(z)$ are equal. As a result the output, the performance and the signals at the internal levels of the modulator are the same as that of the conventional modulator. On the other hand, focusing on the signal at the input of the quantizer, this signal is given by:

$$V_R(z) = [V_Q(s) - V_{Q1}(s)]^* \qquad (4)$$

In the proposed architecture $V_{Q1}(s)$ is derived from V_Q and operates as a good prediction of V_Q. Therefore, the signal range of $V_R(z)$ can be much smaller than the signal range at the input of the modulator. This is the basic idea of the architecture of Fig. 1. Finally, note that their is a similarity with a modulator using a two-step flash. However, in our architecture the input-output delay of the two-step flash and the power hungry analog sample&hold are avoided.

To obtain the prediction signal $V_{Q1}(s)$, $V_Q(s)$ is sampled in a (low-resolution) auxiliary quantizer ($quant_a$ in Fig. 1). Next, $V_{Q1}(s)$ is found by sending this rough estimation of V_Q through an auxiliary DAC. To allow the cascade of auxiliary quantizer, auxiliary DAC and main quantizer to be defined properly, the signal $V_Q(s)$ is sampled on the falling edge of the clock and the signal V_R on the next rising edge.

Fig. 1 showed the conceptual architecture of our modulator, now we turn our attention to the one that was actually implemented, shown in Fig. 2. The same principle of prediction is

1-4244-0395-2/06/$20.00 ©2006 IEEE.

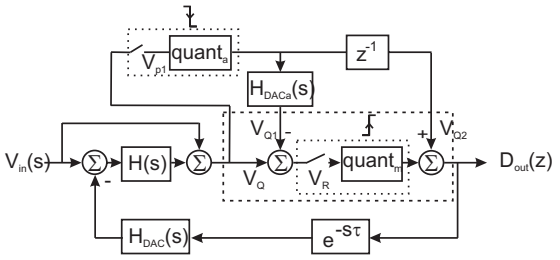

Fig. 1. Modulator architecture.

used to reduce the signal range at the input of the 6-bit main quantizer (with quantization step Δ_m). The auxiliary quantizer is a 3-bit quantizer (with quantization step Δ_a) and the filter is of third order. The adder after the loop filter in Fig. 1 is doubled into two adders (i) and (ii). These add the three output signals of the three integrators to the input signal of the modulator. It can be shown, by theory and by simulations, that the signal range at the input of the quantizer is covered by 10 quantization steps Δ_m. To account for additional parasitic effects like gain and/or offset errors [2], we implemented 14 comparator levels in the main quantizer. Through the use of the interpolation technique, the number of comparators was further reduced to 7 [7]. Together with the 8 comparators of the auxiliary quantizer, a total of 15 comparators were used instead of the 63 required in the conventional modulator.

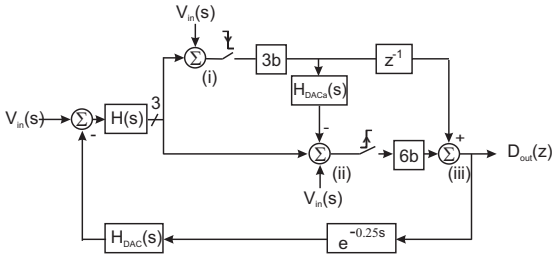

Fig. 2. Implemented modulator.

III. System level design

Observing the input-output behavior of the dashed rectangular in Fig. 1 it can be seen that this behavior is identical to a conventional full-range 6-bit quantizer. Therefore, we could use any known design strategy for a multi bit continuous time $\Sigma\Delta$-modulator. Generally, the design of a continuous time $\Sigma\Delta$-modulator is inspired by the discrete time variant. This means the loop filter $H(s)$ is designed such that the equivalent discrete time loop filter $H_{eq}(z)$ equals a desired discrete time filter say $H_{aim}(z)$. However, both the time required for a DEM technique (e.g. [8]) to linearize the DAC in the feedback path as well as the finite decision time of the quantizer add to an inevitable loop delay. As a consequence if $H(s)$ is of third order, $H_{eq}(z)$ is of fourth order. This means that loop delay causes the described method to be unfeasible and to result in the structure lacking one degree of freedom to have full control over all the poles. This problem has been solved in e.g. [4] by the introduction of an additional feedback path directly to the input of the quantizer. However, in our case this additional path is an (expensive) 6-bit DAC, making this solution less interesting.

Therefore, the loop filter was designed in a different way, using the approach presented by the authors in [3]. The design is based on the Nyquist-curve of the equivalent discrete time loop filter, given by:

$$H_{eq}(z) = \mathcal{Z}\left[\mathcal{L}^{-1}\left(H(s)H_{DAC}(s)e^{-s\tau}\right)\Big|_{t=nT}\right]. \quad (5)$$

Here, τ is the loop delay. Instead of considering this as a parasitic effect, it is included in the nominal design and the value is fixed by the circuit implementation to 25% of the clock period. Next, the three parameters of the third order loop filter were chosen such that the vector gain margin (VGM) of $H_{eq}(z)$ was maximized. This vector gain margin is defined as:

$$VGM = \frac{1}{1 - R_{min}}, \quad (6)$$

where R_{min} is the minimum distance of the Nyquist-curve of $H_{eq}(z)$ to the critical point -1 (see also Fig. 3). It has been shown in [3] that this VGM is a practical way to evaluate the robust stability of the modulator. Therefore, maximizing the VGM maximizes the robust stability of the modulator. This procedure results in the design shown in Fig. 3. On the left the Nyquist-curve of the modulator is shown, it has a VGM of about 2. The right of the figure shows the response of the NTF.

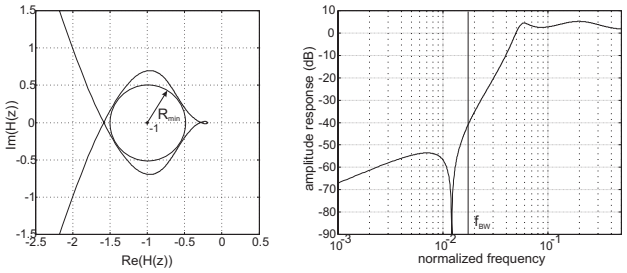

Fig. 3. Detailed image of the Nyquist-curve of $H_{eq}(z)$(left). Amplitude response of the NTF (right).

IV. Circuit level design

The modulator of Fig. 2 was designed in a 0.35 μm CMOS technology with four metal and two poly layers. The supply voltage was 3.3 V. The first integrator in the loop is implemented as an RC-active integrator, using a telescopic cascode operational amplifier. The second and third integrator are implemented as g_mC-integrators with a local feedback path, similar to [5]. For the adders (i) and (ii) (see Fig. 2) simple g_m-cells of which the output current flows through a common resistive ladder are used. In the special case of adder (ii) the prediction signal generated by the auxiliary quantizer is added using a current steering DAC, like shown in Fig. 4 [4]. On the ladder signals can be drawn off at several points. This way the comparator inputs can be tapped directly from

the ladder [4]. In the case of Fig. 4 these points correspond to the 14 comparator levels used in the main quantizer. A comparator consists of a pre-amplifier and a dynamic latch.

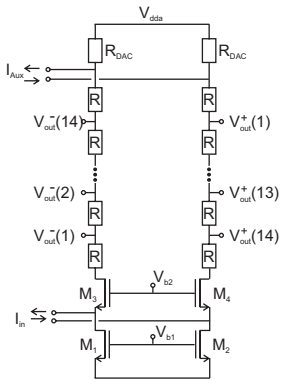

Fig. 4. The resistive ladder of adder (ii) for the main quantizer.

The feedback DAC is linearized using data weighted averaging [8] implemented with transmission gate logic (TMG-logic) [9] in order to limit the delay in the loop. The TMG-logic consists of shifters where a single bit input indicates whether the input code of the shifter should or should not be shifted over a fixed number of positions. In our case each shifter consists of only nMOS-transistors. This is possible, since the default output voltage of the dynamic latches is high and only transitions from high to low should ripple fast through the TMG-structure. TMG-logic was also used to realize a fast implementation of adder (iii).

Next, the output code of the TMG-array is send to an array of latches [10] The clock used for these latches is delayed over 25% of the clock period to set the loop delay in accordance to the system level design.

V. Evaluation

A. Simulations

During the complete design procedure the VGM was used as a key element. It was e.g. used to measure the degradation of the stability of the modulator due to parasitic effects introduced by the actual implementation of the circuit elements. Such an evaluation is illustrated in Fig. 5 and 6. Normally, designers use the Bode-diagram of $H(s)$ like shown in Fig. 5 to evaluate their design by means of e.g. the phase margin. However, in the design of a continuous time $\Sigma\Delta$-modulator the Bode-diagram of $H(s)$ does not include the transfer function of the DAC, $H_{DAC}(s)$. Even if the transfer function of the DAC is included and the Bode-diagram of $H(s)H_{DAC}(s)$ is investigated, still the sampling operation is ignored. Therefore, we used the same data used for the Bode-diagram of Fig. 5 to find the discrete time equivalent loop filter using:

$$H_{eq,sim}(z) = \frac{1}{T}\sum_{n=-\infty}^{n=\infty}\left(H(s+j2\pi f_s)H_{DAC}(s+j2\pi f_s)\right) \quad (7)$$

In practice this infinite sum can be broken up after about 5 terms. Using this $H_{eq,sim}(z)$ both the transfer function of the DAC as well as the sampling operation are included in the analysis.

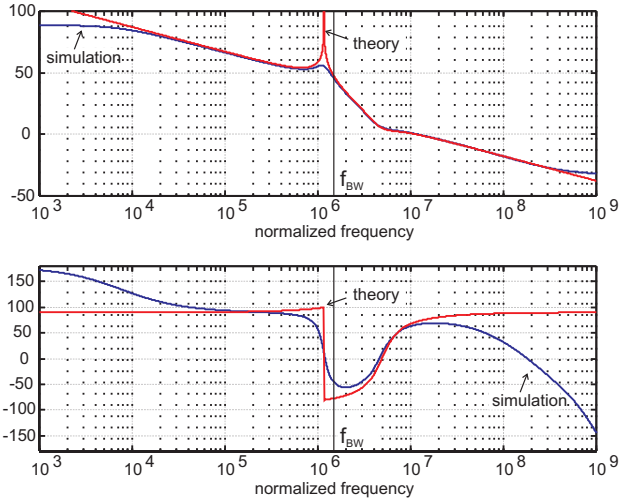

Fig. 5. Bode-diagram of the loop filter $H(s)$ at the system level and in simulation.

The (robust) stability of the modulator is next checked using the VGM using the Nyquist curve of $H_{eq,sim}$ like shown in Fig. 6. This figure also includes a comparison with the Nyquist curve at the system level $H_{eq}(z)$. Based upon this figure it is concluded that due to the parasitic effects the VGM of the simulated modulator including all but the layout parasitics is reduced from 2.03 to 1.82. This measure leaves enough margin for the modulator to be robust against other (unsimulated) parasitics and/or parameter uncertainties. Especially the latter might be important since the first integrator is of a different type compared to the last two and since no tuning mechanisms were included.

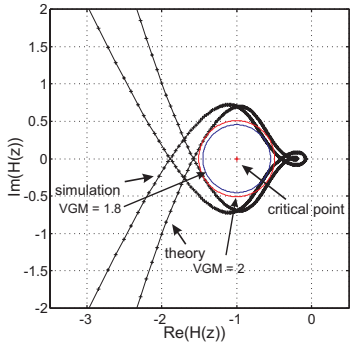

Fig. 6. Comparison of the Nyquist-curve of the discrete time equivalent loop filter $H_{eq}(z)$ at the system level and in simulation.

B. Measurements

A microscopic photo of the chip with the main circuit components indicated is shown in Fig. 7. Including the pads the chip is about 3.61 mm^2 large, the core 1.44 mm^2. The prototype was packaged in a standard 44-pins JLCC package. For the measurements it was socketed on an FR4 four layer

TABLE I

THE MAIN CHARACTERISTICS OF THE PROTOTYPE.

Technology	0.35 μm CMOS (4M2P)
Supply voltage	3.3 V
Clock frequency	192 MHz
Sampling frequency	96 MHz
Bandwidth after reconstruction	1.5 MHz
Measured power consumption	54 mW Analog
	17 mW Clock amplifiers and buffers
Peak SNDR	76 dB
Peak SNR	82 dB
Dynamic range	85 dB

test board. A bandwidth of 1.5 MHz was targeted, leading to a sampling frequency of 96 MHz with an OSR of 32. To realize the 25% delay in the loop the applied clock frequency was 192 MHz. A clock amplifier on the chip can produce four clock phases (having a phase shift of 0, 25%, 50% and 75%) out of a low-level sinusoïdal RF input signal.

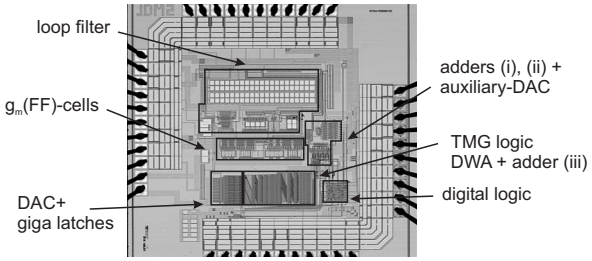

Fig. 7. Microscopic photo of the chip.

Preliminary test results are presented in this paper, starting with the measurement result of Fig. 8. It shows the baseband spectrum for a 100 kHz sine wave input signal with an amplitude of 3.5 dB below the full scale. The measured SNR and SNDR as a function of the input amplitude is shown in Fig. 9. It exhibits a drop around -15 dB. The origin of this drop is still uncertain but is probably due to the speed of adder (ii). This adder's speed is lower than expected due to underestimated layout parasitic capacitances. The main characteristics of the chip are summarized in table I.

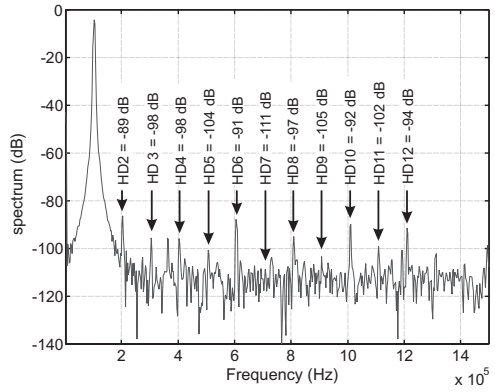

Fig. 8. Spectrum of decimated signal.

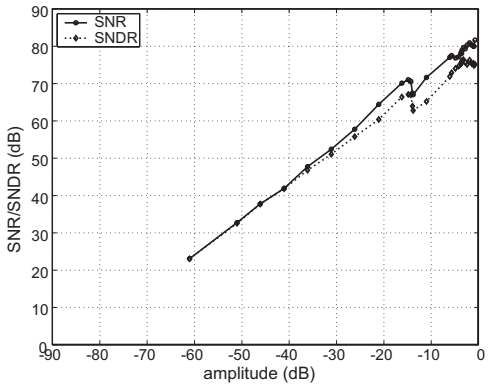

Fig. 9. SNR and SNDR as a function of the input amplitude (dB).

VI. CONCLUSION

In this paper we presented a design of a continuous time $\Sigma\Delta$-modulator. It uses a 6-bit internal quantizer while only requiring a total of 15 comparators. The design of the modulator was based on the Nyquist stability criterion and the vector gain margin.

ACKNOWLEDGMENT

J. De Maeyer is supported by a fellowship of the Fund for Scientific Research - Flanders (F.W.O.-V., Belgium). He is currently with AMISemiconductor Belgium, Oudenaarde, Belgium.

REFERENCES

[1] S. Yan and E. Sánchez-Sinencio, "A Continuous-Time $\Sigma\Delta$ Modulator With 88-dB Dynamic Range and 1.1-MHz Signal Bandwidth," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 75–86, Jan. 2004.

[2] J. De Maeyer, S. Reekmans, P. Rombouts, and L. Weyten, "Multibit Continuous Time $\Sigma\Delta$ Modulators with a Reduced Number of Comparators," *WSEAS Trans. Circuits and Systems*, vol. 3, no. 9, pp. "1781–1786", Nov. 2004.

[3] J. De Maeyer, P. Rombouts, and L. Weyten, "Nyquist Criterion based Design of Continuous Time $\Sigma\Delta$ Modulators," in *Proc. IEEE Int. Symp. on Circ. and Syst. (ISCAS)*, Kos, Greece, May. 2006, accepted for publication.

[4] S. Patón, A. Di Giandomenico, L. Hernàndez, A. Wiesbauer, T. Pötscher, and M. Clara, "A 70-mW 300-MHz CMOS Continuous-Time $\Sigma\Delta$ ADC with 15-MHz Bandwidth and 11 Bits of Resolution," *IEEE J. Solid-State Circuits*, vol. 39, no. 7, pp. 1056–1063, Jul. 2004.

[5] E.J. van der Zwan, K. Philips, and C.A.A. Bastiaansen, "A 10.7-MHz IF-to-Baseband $\Sigma\Delta$ A/D Conversion System for AM/FM Radio Receivers," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1810–1819, Dec. 2000.

[6] J. De Maeyer, J. Raman, P. Rombouts, and L. Weyten, "Controlled Behavior of the STF in CT $\Sigma\Delta$ Modulators," *IEE Electronics Letters*, vol. 41, no. 16, pp. 19–20, Aug. 2005.

[7] P. Vorenkamp and R. Roovers, "A 12-b, 60-MSample/s Cascaded Folding and Interpolating ADC," *IEEE J. Solid-State Circuits*, vol. 32, no. 12, pp. 1876–1886, Dec. 1997.

[8] R.T. Baird and T.S. Fiez, "Linearity Enhancement of Multibit $\Delta\Sigma$ A/D and D/A Converters Using Data Weighted Averaging," *IEEE Trans. Circuits & Systems-II*, vol. 42, no. 12, pp. 753–762, Dec. 1995.

[9] M. Miller and G. Petrie, "A Multibit Sigma-Delta ADC for Multimode Receivers," *IEEE J. Solid-State Circuits*, vol. 38, no. 3, pp. 475–782, Mar. 2003.

[10] A. Van den Bosch, M.A.F. Borremans, M.S.J. Steyaert, and W. Sansen, "A 10-bit 1-GSample/s Nyquist Current-Steering CMOS D/A Converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 315–324, Mar. 2001.