ECRL_2 as one ADVSL gate can implement complex, high fan-in logic function. The power of ADVSL is also reduced greatly compared to the conventional CMOS and ECRL adder. At 20 MHz, the power of ADVSL is only 10.6% of the conventional CMOS power, and at 50 MHz, the ADVSL power is only 22.1% of the conventional CMOS power. ADVSL loss is only 30.7% of ECRL_2 loss at 20 MHz, and 41.7% of ECRL_2 loss at 50 MHz. As ECRL_1 takes the same architecture of the ADVSL adder, its gate count and transistor count are also reduced greatly. However ECRL_1 power is not reduced, but rather increased greatly compared to ECRL_2, because the complex logic make the trapped charges of internal nodes increase sharply.

Conclusions: A new adiabatic logic (ADVSL) is presented. It reduces trapped charges in internal nodes greatly, energy-efficiently implementing complex high fan-in logic in a single gate. The dissipation of an adiabatic system, taking the architecture based on a relatively small number of complex ADVSL gates, can be reduced significantly.

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References

1 Lim, J., Kim, D.G. Kim, D.G., and Chae, S.I.: 'nMOS reversible energy recovery logic for ultra low energy applications', *IEEE J. Solid-State Circuits*, 2000, **35**, (6), pp. 865–875
2 Moon, Y. and Moon, Y., and Jeong, D.K.: 'An efficient charge recovery logic circuit', *IEEE J. Solid-State Circuits*, 1996, **31**, (4), pp. 514–522
3 Hung, P.C. and Hung, P.C., and Wang, I.H.: 'Complementary pass-transistor energy recovery logic for low-power applications', *IEE Proc., Comput. Digit. Tech.*, 2002, **149**, (4), pp. 146–151
4 Knapp, M.C., Kindlmann, P.J., and Papaefthymiou, M.C.: 'Design and evaluation of adiabatic arithmetic units', *Analog Integr. Circuits Signal Process.*, 1997, **14**, pp. 71–79

Sixth-order programmable bandwidth bandpass sigma–delta modulator implemented with transmission lines

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An implementation of a sixth-order bandpass continuous time sigma–delta modulator using transmission lines is presented. A single tuning coefficient allows the exchange of resolution and bandwidth in this modulator, owing to the use of a two path transformation that exploits the similarity between transmission line modulators and discrete time modulators. The modulator tolerates two clock cycles of excess loop delay and a high clock jitter.

Introduction: The coexistence of different communication standards in wireless systems demands new data converter architectures that allow reconfiguration to exchange bandwidth by resolution. Two common ADC converter architectures for digital receivers are pipeline converters and continuous time sigma–delta modulators (CTSD) [1]. The coefficients of the loop filter of a CTSD modulator are dictated by the sampling period, which complicates bandwidth programmability by changing the clock frequency. Alternatively, pipeline converters do not employ noise shaping and, hence, cannot improve significantly their resolution by oversampling signals of different bandwidths.

We present a bandpass sigma–delta modulator that benefits from the hardware implementation of continuous time modulators while preserving the advantages of discrete time modulators (DTSD), such as reduced jitter sensitivity. This modulator is based on similar principles to the lowpass modulator described in [2] and uses transmission lines as delay elements. The novelty of the modulator presented here, compared to [2], is the use in the design of its equivalent discrete time NTF of a z^{-1} to z^{-2} transformation, known as two-path transformation [3]. This allows us to trade off analogue signal bandwidth by resolution with a single tuning coefficient. As an additional benefit, the modulator tolerates two full clock periods of excess loop delay and a higher clock jitter level than conventional continuous time band pass modulators. Note that an N-path transformation is feasible in a delay-based CTSD modulator [2] owing to its formal similarity to discrete time modulators. An equivalent approach is not easily feasible in continuous time modulators based on lumped elements.

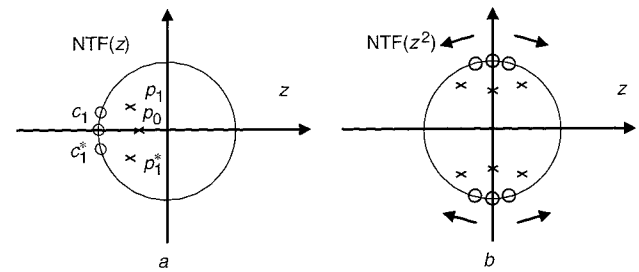

Fig. 1 *Prototype NTF pole-zero plots*
a Pole-zero plot of NTF(z) prototype used in design
b Effect of replacing z^{-1} by z^{-2} in the NTF

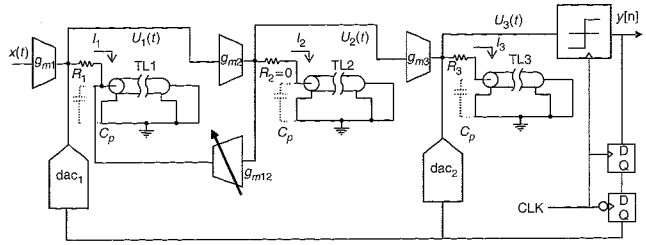

Fig. 2 *Block diagram of modulator*

Design: Fig. 1*a* depicts the pole-zero plot of the NTF(z) prototype that will be used in the design. This transfer funcion has two complex conjugate zeros located in the unit circle close to a real zero at $z=-1$. The phase $\pm\phi$ of the two complex conjugate zeros will define the bandwidth of interest of the modulator and will be selected according to the desired oversampling ratio R. The NTF has been equipped also with three poles p_0, p_1 and p_1^* to provide stability in a single bit design. If we replace z^{-1} by z^{-2} in the NTF, the zeros and poles are shifted around $z=e^{\pm\pi/2}$ and the order is doubled, as shown in Fig. 1*b*, without an increase in the resonator count. The expression for the NTF represented in Fig. 1 is as follows:

$$\mathrm{NTF}(z)=\frac{(z^2+1)(z^4-2\cos(\phi)z^2+1)}{(z^4+az^2+b)(z^2-c)} \tag{1}$$

The next step in the design is to accomplish the block diagram of a delayed system [2] with an equivalent behaviour to the proposed discrete time modulator. We may implement such a retarded system by means of transconductors, transmission lines, a sampler and quantiser and two current feedback DACs. The proposed system is shown in Fig. 2, where all transmission lines TL are identical, have a characteristic impedance Z_0, an electrical delay T corresponding to the sampling frequency period $f_s=1/T$, and a loss parameter $A\leq 1$. It may be shown that any of the state variables u_i comply with the following relationship

$$U_i(s)=\left(R_i+Z_0\frac{1-Ae^{-s2T}}{1+Ae^{-s2T}}\right)I_i(s) \tag{2}$$

Considering the system equivalence defined in [2], we may replace e^{-s2T} by z^{-2} in (2) and compute the corresponding NTF and STF of the modulator as if it were a discrete time system. Note that the equivalence in [2] holds for any DAC pulse shape of finite duration T, because the value of the DAC pulse in the sampling instant is what is relevant instead of the pulse area, as opposed to a conventional CTSD. We will select a NRZ zero-order-hold pulse which will desensitise the modulator against clock jitter and excess loop delay, owing to its constant value over the sampling period. To complete the design, it suffices to equate the coefficients of (1) with the NTF(z) obtained using Fig. 2 and (2) (assuming $A=1$) and the proposed replacement.

Transconductances g_{m1}, g_{m2} and g_{m3} may be considered design parameters to scale the state variables $u_i(t)$ and the STF gain. Table 1 shows the resulting design equations.

Table 1: Design equations

$dac_1 = \frac{1-b+ac-2\cos^2(\phi)+(bc-a+c)\cos(\phi)}{2Z_0^2 g_{m_1} g_{m_3}(2\cos(\phi)-1-\cos^2(\phi))}$	
$dac_3 = \frac{3-a-b+c+bc+ac-4\cos(\phi)}{4Z_0(\cos(\phi)-1)}$	
$R_1 = Z_0 \frac{(2\cos(\phi)-c+bc+a)(\cos(\phi)-1)}{1-b+ac-2\cos^2(\phi)+(bc-a+c)\cos(\phi)}$	
$R_2 = 0$	$R_3 = Z_0$
$g_{m_{12}} = -\frac{1+\cos(\phi)}{Z_0^2 g_{m2}(1-\cos(\phi))}$	

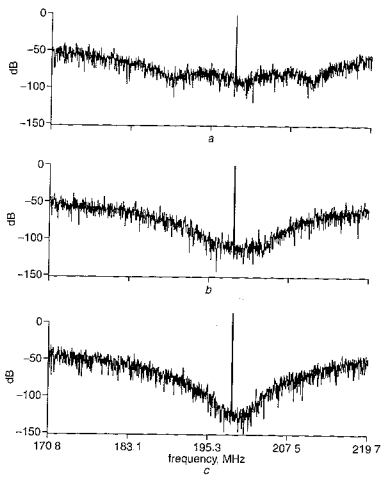

Fig. 3 *FFT of time domain simulations with different values of g_{m12}*
a $R=16$ b $R=128$ c $R=256$

Table 2: Circuit parameters

$g_{m1}=3.4$ mA/V	$g_{m2}=6.8$ mA/V	$g_{m3}=3.4$ mA/V
$R_1=586\ \Omega$	$R_2=0$	$R_3=50\ \Omega$
$dac_1=\pm 367\ \mu$A		$dac_3=\pm 1.05$ mA

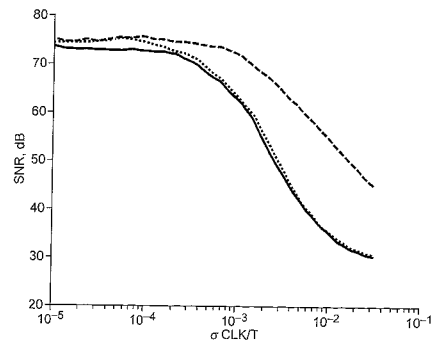

Fig. 4 *SNR against clock jitter variance*

The signal bandwidth of the modulator depends on angle ϕ and can be modified by transcondutance g_{m12}, which moves four of the zeros of Fig. 1*b* all together, as shown by the arrows. Setting constant values for dac_1, dac_3 and R_1 and changing only g_{m12} shifts also the location of the NTF poles. However, as ϕ approaches π this pole shift is small enough for the modulator to remain stable, as will be verified by simulaton in the next section.

The NTF expressed in (1) requires a loop with a z^{-2} delay block. This is equivalent to delaying the quantiser data by two clock cycles before reaching the feedback DAC. The feedback path in Fig. 3 contains a quantiser and two D flip–flops triggered in the rising and falling edges of the sampling clock respectively. For a symmetric clock signal, this configuration would update the DAC output with the data captured in the quantiser 1.5 clock cycles before. The next sampling operation in the quantiser would occur 0.5 clock cycles after the DAC update. Hence, this circuit provides the two clock cycles of delay required by the NTF and forces the sampler to sample in the middle of the zero-order hold feedback DAC pulse. By doing so, the modulator is desensitised from clock jitter or code dependent distortion of the DAC pulses, which will accumulate in the DAC pulse edges.

Simulations: To prove the validity of this design we have used the model in Fig. 2 to simulate the system along with some circuit nonidealities. To define a practical case, we use the circuit parameters shown in Table 2, a line impedance of 50 Ω, an input full scale 0 dB_{fs} = −10 dBm and a sampling frequency $f_s = 800$ MHz.

Fig. 3 shows the fast Fourier transforms (FFT) of three time domain simulations of the same modulator using nonideal transconductors with a bandwidth limitation by a dominant pole at 3fs, transmission lines with a loss parameter $A=0.97$ (see (2)) and a parasitic capacitor $C_P=2$ pF, as shown in Fig. 2, representing the pad capacity of a possible implementation with off-chip resonators. This parasitic capacitor forces us to reduce the line delay by the time constant $\tau = C_P Z_0$ to equalise the impulse response of the line at the sampling points. The simulations use three values of g_{m12}, computed by optimising the NTF for oversampling ratios $R=16$, 128 and 256, respectively. Fig. 4 shows the maximum SNR of three modulator configurations when the clock source has a Gaussian jitter of increasing standard deviation, considering an oversampling $R=128$. The solid trace in Fig. 4 corresponds to the modulator used in Fig. 3. The dotted trace in Fig. 4 represents the same modulator as in the solid trace but with ideal transconductors. As may be seen, a bandwidth of 3fs is enough to guarantee similar jitter performance as for the ideal case. The dashed trace in Fig. 4 has been included as a reference and represents the SNR of a DTSD modulator equivalent to the modulator in Fig. 2, where clock jitter only affects the input signal sampler.

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References

1 Li, X., and Ismail, M.: 'Multi-standard CMOS Wireless Receivers. Analysis and Design' (Kluwer Academic Publishers, Boston, MA, 2002)
2 Hernandez, L.: 'Continuous-time sigma-delta modulators with reduced timing jitter sensitivity based on time delays', *Electron. Lett.*, 2003, **39**, (14), pp. 1039–1041
3 Ong, A.K., and Wooley, B.A.: 'A two-path bandpass ΣΔ modulator for digital IF extraction at 20 MHz', *IEEE J. Solid-State Circuits*, 1997, **32**, (12), pp. 1920–1934

Temperature dependence of type I-IA dual-fibre Bragg gratings

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Fibre Bragg gratings (FBGs) of a new IA type have been reported to show thermal behaviour that is different from that of conventional type I gratings. Given a sufficiently large temperature coefficient difference between the two grating types, a dual-grating sensor formed by both types of gratings could allow simultaneous temperature and strain measurement. Such dual-grating sensors were prepared for the 830 nm wavelength region and tested at temperatures of up to 300°C. As far as the variation of the different temperature coefficients is concerned, the temperature coefficient of type IA FBGs and the temperature coefficient of type I FBGs have been found to converge as the temperature increases. The difference in temperature coefficients drops to 1% after annealing at 300°C.