

DOUBLE-SAMPLING $\Sigma\Delta$ ADC'S WITH BILINEAR INTEGRATORS.

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Abstract : Double-sampling allows to double the sampling frequency of a $\Sigma\Delta$ ADC without increasing the clock frequency. Unfortunately, path mismatch between the double-sampling branches causes noise folding, which ruins the performance. The fully-floating integrator is an interesting circuit to be used in such a double-sampling $\Sigma\Delta$ ADC because it is tolerant to path mismatch. However, this circuit exhibits an undesired bilinear filter effect, which effectively increases the order of the modulator by one. Due to this, previously presented structures don't have enough freedom to fully control the modulator pole positions. In this work we introduce modified topologies for double-sampling $\Sigma\Delta$ -modulators with bilinear integrators. We show that these architectures provide full control of the modulator poles and hence can be used to implement any noise transfer function.

Key Words : $\Sigma\Delta$ Modulation, ADC, double-sampling, switched-capacitors

1 Introduction

Double-sampling is a technique that makes switched capacitor circuits update their output during both clock phases of the clock. This way, a sampling frequency twice the clock frequency is achieved [1–5]. When this technique is employed in $\Sigma\Delta$ modulation ADC's this could lead to considerably higher performance.

Unfortunately, double-sampling $\Sigma\Delta$ -modulator ADC's are sensitive to path mismatch, which causes quantization noise to fold from the Nyquist frequency into the signal band. In this work, we focus on the use of bilinear integrators [3–5] to reduce the effect of noise folding. If such a bilinear integrator uses a so-called fully-floating input branch, its operation is nearly unaffected by path mismatch [4, 5], making it a promising candidate to implement a double-sampling $\Sigma\Delta$ modulator.

In the following we shall show that the pres-

ence of the bilinear transfer function in the loop increases number of modulator poles by one. Due to this, in previously presented modulators the pole positions could not be controlled fully. In section 4 we introduce novel architectures that allow full control of the modulator pole positions, and demonstrate that they can be used to design greatly improved $\Sigma\Delta$ modulators.

2 Double-sampling and noise folding

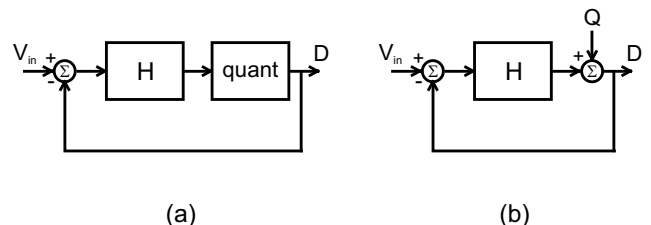


Fig. 1. Conceptual diagram of a $\Sigma\Delta$ modulator and its linearized model.

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Fig. 1(a) shows a conceptual diagram of a $\Sigma\Delta$ modulator. It consists of a feedback loop with a loop-filter H and a quantizer. To analyze this system it is common to model the quantizer as an additive error Q , as shown in Fig. 1(b). Hence, the digital output D can be obtained as:

$$D(z) = \text{STF}(z)V_{in}(z) + \text{NTF}(z)Q(z). \quad (1)$$

Here $\text{STF}(z)$ corresponds to the signal transfer function and $\text{NTF}(z)$ to the noise transfer function. In practical modulators the STF will be close to unity in the signal band.

If such a modulator uses double-sampling, an additional (undesired) noise term will appear in the output signal. We will call this additional noise contribution the folded noise N_{fold} .

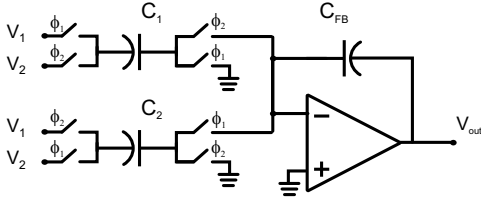


Fig. 2. Conventional double-sampled integrator circuit.

The main building block in a $\Sigma\Delta$ modulator is an integrator. A conventional two-input double-sampled integrator is shown in Fig. 2. It consists of an operational amplifier with a fixed feedback capacitor C_{FB} and two matched switched input capacitors C_1 and C_2 . Due to the interleaved operation of both capacitors, the output voltage is updated on both clock phases ϕ_1 and ϕ_2 . Thus the sampling frequency equals twice the clock frequency. If both capacitors C_1 and C_2 are perfectly matched, this circuit performs a two-input integration where the input V_1 is delayed and integrated and the input V_2 is inverted and undelayed integrated. By setting V_1 or V_2 to ground, either a delaying or non-delaying integration can be implemented. This signal flow operation is shown in Fig. 3(a), where the coefficient $a = C_1/C_{FB}$.

Unfortunately, the capacitors C_1 and C_2 can not be matched with infinite precision. Let us therefore introduce the path mismatch $\delta = (C_1 - C_2)/(C_1 + C_2)$. The effect of this path mismatch is

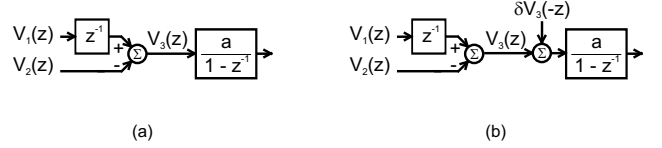


Fig. 3. Equivalent diagram of the double-sampled circuit (a) without path mismatch and (b) with path mismatch.

an amplitude modulation (AM) with half the sampling frequency f_S . Such an AM corresponds to a frequency translation and is called folding. This effect can be analyzed in a very similar way as in [1], to show that it can be modelled by adding an additive contribution $V_{eq}(z)$:

$$V_{eq}(z) = \delta V_3(-z). \quad (2)$$

Here V_3 is defined by the diagram in Fig. 3(a). This results in the model shown in Fig. 3(b).

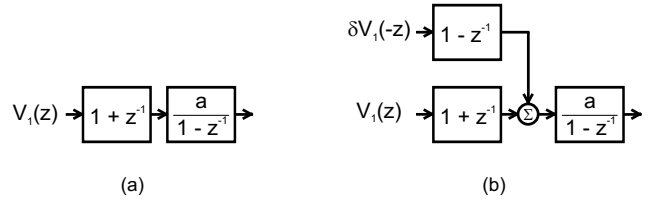


Fig. 4. Equivalent diagram of a bilinear double-sampled circuit (a) without path mismatch and (b) with path mismatch.

A particularly relevant case occurs when $V_2 = -V_1$. Then we obtain a bilinear double-sampled input circuit. The corresponding diagram is shown in Fig. 4(a). The diagram for the case with path mismatch is shown in Fig. 4(b). As shown in this figure, the folding mechanism exhibits a first-order differentiation, as was already shown in a different way in [3]. Note that inverted signal levels are readily available in any fully differential circuit, and hence such a bilinear circuit can be implemented easily.

An alternative double-sampled implementation of a bilinear integrator is shown in Fig. 5 [4]. It is based on a so-called fully-floating input branch, which consists of the switched capacitors C_A and C_B . It can readily be derived by inspection that this circuit indeed performs a bilinear integration

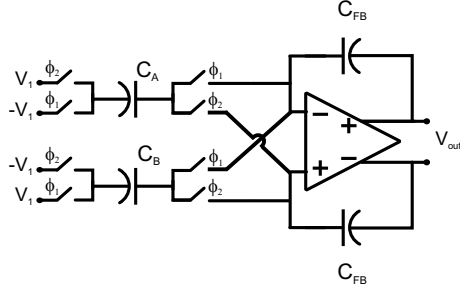


Fig. 5. Fully floating bilinear integrator circuit.

with an output $V_{out}(z) \sim (1+z^{-1})/((1-z^{-1}))V_1(z)$. It was shown in [4] that mismatch between the capacitors C_A and C_B has no effect on the operation of this circuit. Hence there is no folding effect from this input, which makes it a particularly attractive circuit for use in a double-sampling $\Sigma\Delta$ ADC. A drawback of this circuit is that there is no DC path toward the input nodes of the operational amplifier. Hence its input common mode voltage is not defined. As such this circuit can not function in reality.

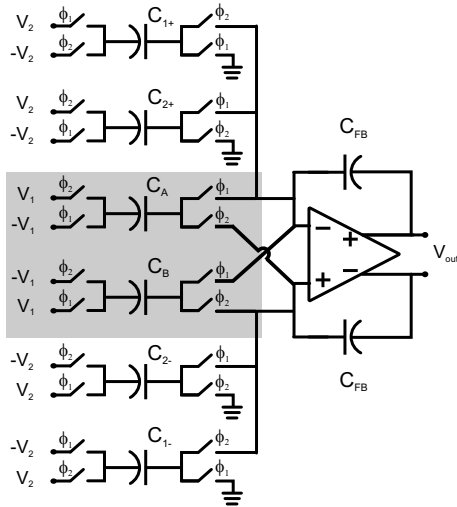


Fig. 6. Two-input bilinear integrator circuit.

A simple way to overcome this problem is to add a conventional non-floating input branch to the integrator [4]. This additional input may be bilinear or not. The bilinear case is shown in Fig. 6. In this adapted circuit the fully-floating input branch (connected to V_1) is still unaffected by path mismatch, but the non-floating input branch (connected to V_2) will be affected in the same way as for the circuit of Fig. 2.

3 Prior $\Sigma\Delta$ modulators with double-sampling bilinear integrators

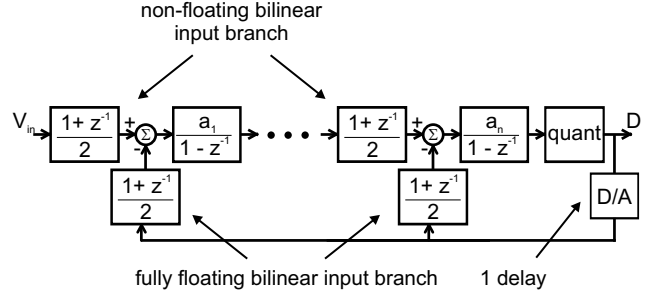


Fig. 7. Double-sampled $\Sigma\Delta$ modulator of [4]

In [4] the architecture of Fig. 7 was introduced. It consists of a cascade of n bilinear integrator circuits of Fig. 6. In the diagram, the bilinear transfer functions have an additional division by 2 such that they equal unity in the lowpass baseband ($z \approx 1$). This way the resemblance with conventional (non-bilinear) structures becomes evident. As indicated in the figure, the fully-floating input is used for the feedback branch, while the non-floating branch is used for the other integrator input. Note that the combination of the quantizer and the feedback D/A conversion also introduces 1 delay, which we will allocate to the DAC.

This structure realizes an NTF with n zeros in the lowpass baseband. One drawback of this structure is that the modulator has $n + 1$ poles. This is obvious from the fact that the main feedback loop exhibits $n + 1$ delays. This implies that the corresponding NTF will take the following form:

$$\text{NTF} = \frac{z(z-1)^n}{P(z)}. \quad (3)$$

here $P(z)$ is a polynomial of order $(n+1)$. Unfortunately, this structure only provides n independent degrees of freedom (the values of the n a_i -coefficients) to control the $(n + 1)$ poles. This implies that it is impossible to properly control the NTF. As a result, the synthesis of high-order modulators is unpractical. This way, this topology has only been reported for modulator loops with $n = 2$ bilinear integrators [4].

In [4], it was already demonstrated that this structure is nearly not affected by noise folding,

however no analysis of the residual folded noise was given. To do this, we first notice that the paths with fully-floating branches don't introduce noise-folding. Folding of the input-signal does not affect the performance either, because the input-signal normally does not have spectral content near half the sampling frequency [2, 4, 5]. Hence, the first integrator in the cascade where folding influences the performance is the second one. To study this, the equivalent diagram of Fig. 4(b) can be inserted for this integrator. Doing this, and after performing some algebraic manipulation it can be shown that the folded noise $N_{fold}(z)$ can be approximated as:

$$N_{fold}(z) \approx \delta z^{-1} Q(-z) \text{NTF}(-z) \left(\frac{1 - z^{-1}}{1 + z^{-1}} \right)^3 \quad (4)$$

Apart from the third-order differentiation, all factors in the above expression are finite and nonzero for $z \approx 1$. Hence, we can observe that the effect of path mismatch will be greatly suppressed.

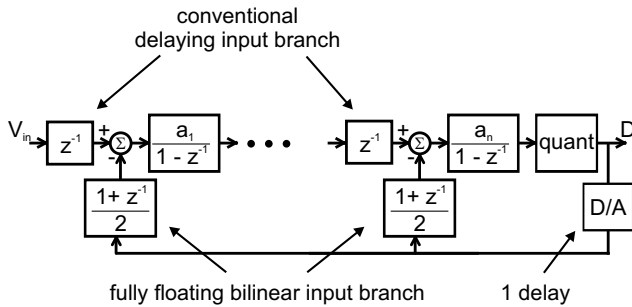


Fig. 8. Double-sampled $\Sigma\Delta$ modulator of [5]

An alternative known architecture is shown in Fig. 8 [5]. Here all the integrators have a fully-floating bilinear input branch for the feedback signal. But the non-floating input of each integrator is non-bilinear. For n baseband zeros, this structure exhibits $n + 1$ delays in the main feedback loop as well and hence is of order $n + 1$. Still there are only n independent variables to control the positions of the $(n + 1)$ poles. Again, this means that there is no complete control over the pole positions of the modulator. Just as for the previous structure, until now only modulators with $n = 2$ integrators have been reported.

Also here, the second integrator's input sam-

pling will be the source of the dominant noise folding mechanism. Similarly as for the structure of Fig. 7, noise-folding can be investigated here by introducing the model of Fig. 3 and doing the required manipulations. This way the folded noise is obtained as:

$$N_{fold}(z) \approx \delta \text{NTF}(-z) Q(-z) \frac{(1 - z^{-1})^2}{2z^{-1}(1 + z^{-1})} \quad (5)$$

Again all the factors in the above expression are finite for $z = 1$, hence a 2nd order differentiation of the effect of path mismatch is observed. While the suppression of noise folding for this structure is inferior to that of Fig. 7, in most applications its effect will be insignificant.

4 Improved Structures

4.1 Modulator architecture

The structures of the previous sections were demonstrated to be quite effective in the reduction of the effect of noise folding. However, they suffer from poor controllability of the modulator pole positions, which makes it unpractical to synthesize high-order modulator loops. In this section we shall introduce 3 improved structures that allow full control of the modulator poles. This enables easy design of high-order modulators with their associated advantages in terms of noise-shaping.

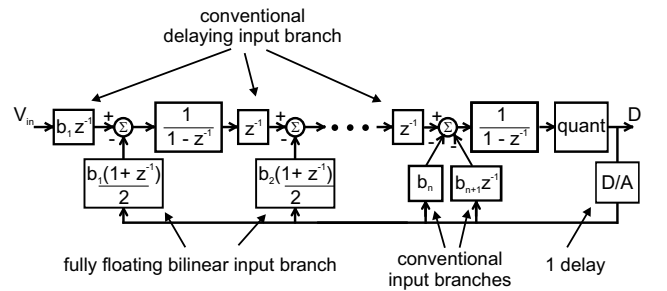


Fig. 9. Architecture with sufficient degrees of freedom to set the poles.

A first improved structure is introduced in Fig. 9. It consists of n integrators. All the n integrators have a conventional delaying input branch which is connected to the previous stage. However, only the first $(n - 1)$ integrators have a fully floating

bilinear input to which the feedback signal is applied. In the last integrator of the chain, the feedback signal is applied through a conventional input branch and also through an additional delaying input branch. This additional delay can easily be implemented in the digital domain, without increasing the complexity of the analog circuit.

By inspection, it can be shown that this structure has an NTF of the form of Eq. (3) and hence, has $(n + 1)$ poles. However now, there are also $(n+1)$ independent degrees of freedom to locate these poles at designed positions, which opens the possibility of easy high-order modulator design.

If the number of integrators n is larger than 2, the dominant noise folding mechanism is identical to that of the structure of Fig. 8. Hence the folded noise is given by Eq. (5), and exhibits a 2nd order differentiation.

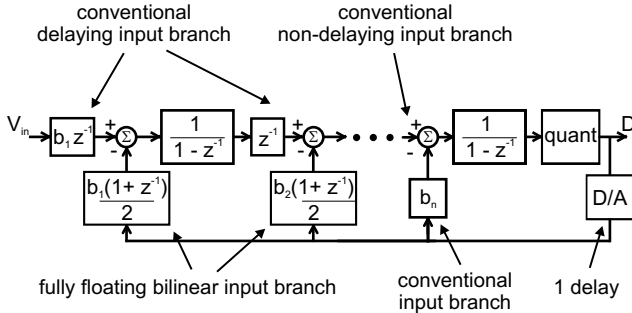


Fig. 10. Double-sampling architecture with only n poles

An alternative structure is shown in Fig. 10. Again it consist of n integrators, where the first $(n - 1)$ integrators have a conventional delaying input and a fully floating bilinear input branch for the feedback signal. However the last integrator in the chain is nondelaying and has only one conventional input branch for the feedback signal. By inspection, it can be concluded that this modulator is now only of n th order, and has n independent degrees of freedom to set the poles.

If the number of integrators is larger than 2, the dominant noise folding is the same as for the structures of Figs. 8 and 9 and given by Eq. (5).

Another alternative is shown in Fig. 11. Here all the n integrators have a conventional delaying input and a fully-floating bilinear input for the feedback signal. This way, this structure has $n + 1$

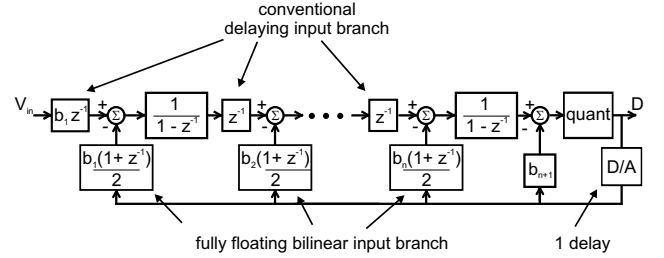


Fig. 11. Alternative architecture with sufficient degrees of freedom to set the poles.

poles. To introduce an additional degree of freedom an additional input branch to the quantizer is added. After analyzing the effect of noise folding, it can be shown that the folded noise in this structure is given by Eq. (5) independently of n , and hence exhibits a 2nd order differentiation of the folded noise.

4.2 Design strategy

Each of the above structures allows full control of its pole positions. This means that these can be set to designed positions.

Traditionally, the design of a $\Sigma\Delta$ modulator focusses on the NTF, and consists of two steps. In a first step, the NTF is synthesized and in a second step this noise transfer function is mapped toward a modulator structure. If we apply this to our case of double-sampling modulators with bilinear feedback, it is clear that the structure of Fig. 10 has n poles and zeros and n independent degrees of freedom. This way, it is fully compatible with any common design strategy. The structures of Figs. 9 and 11 have an NTF of the form of Eq. (3) with $(n + 1)$ poles, n baseband zeros and 1 zero at $z=0$. The simplest design-approach in this case is to set one of the modulator poles equal to $z = 0$. Then, this pole cancels the zero at $z = 0$ and the effective order of the NTF is reduced to n . Hence, these structures can be used with conventional modulator synthesis techniques as well.

Such modulator synthesis strategies often place the NTF-poles in Butterworth configuration [6]. Moreover, also the NTF-zeros may be optimized [6]. To implement this, the architectures of Figs. 9-11 have to be adapted with local feedback of two successive integrators as shown in Fig. 12.

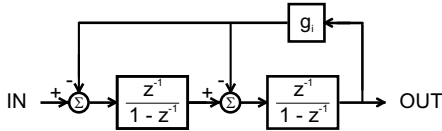


Fig. 12. Resonator with a transfer function $\sim \frac{z^{-2}}{1-z^{-1}(2-g)+z^{-2}}$ based on local feedback of delaying double-sampled integrator circuits.

4.3 Design Example

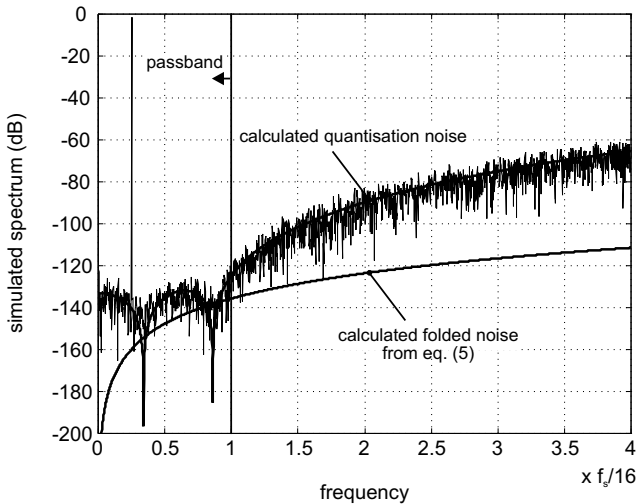


Fig. 13. FFT of simulated double-sampling 4th-order 5-bit modulator

To illustrate the above described approach, a fourth-order 5-bit modulator was designed for an oversampling ratio of 16 as an example. First the NTF was synthesized according to [6] where $\|H\|_2 = 3$ was used as the stability criterion. Then this NTF was mapped toward the structure of Fig. 9, adapted with local feedback as shown on Fig. 12.

Next, a time domain simulation of the resulting structure was performed, where all the double-sampled branches were arbitrarily assigned a path mismatch of $\pm 1\%$. Here the multi-bit dac's were assumed to be linear. In practice, a dynamic element matching technique would be needed to linearize these DAC's [5]. A typical FFT-result for a -1.5 db (relative to full scale) input signal is shown on Fig. 13. The corresponding SNR is 104 dB. The calculated folded noise and shaped quantization noise are shown as well. From the comparison between the calculated and simulated curve it

is clear that the folded noise does not affect the performance even for this case of a large path mismatch (1% as mentioned above).

5 Conclusion

We have shown that existing topologies for double-sampling $\Sigma\Delta$ modulators with bilinear feedback, don't have enough freedom to allow full control of the modulator pole positions. This makes it unpractical to synthesize high-order modulator loops. Next, we have introduced novel architectures that have enough freedom for full control of all the modulator pole positions and have shown that high-order modulators can easily be implemented with these structures. The effectiveness of the proposed approach was confirmed through simulation.

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