Reconfigurable Hardware for a Scalable Wavelet Video Decoder and its Performance Requirements

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Abstract. Multimedia applications emerge on portable devices everywhere. These applications typically have a number of stringent requirements: (i) a high amount of computational power together with real-time performance and (ii) the flexibility to modify the application or the characteristics of the application at will. The performance requirements often drive the design towards a hardware implementation while the flexibility requirement is better served by a software implementation. In this paper we try to reconcile these two requirements by using an FPGA to implement the performance critical parts of a scalable wavelet video decoder. Through analytical means we first explore the performance and resource requirements. We find that modern FPGAs offer enough computational power to obtain real-time performance of the decoder, but that reaching the necessary memory bandwidth will be a challenge during this design.

1 Introduction

When designing a new multimedia system one would usually prefer to implement most of the functionality in software running on a general purpose processor. This improves the ease and flexibility of the design process and avoids the high cost of designing an ASIC. Still, often the performance requirements of the multimedia system are such that specific hardware is necessary. Then again, ASICs do not offer flexibility of the functionality after implementation. For example, an ASIC designed for doing JPEG compression utilizing Huffman encoding will become useless when application changes require arithmetic encoding. This generally results in an overdimensioning of the ASIC so that it can accommodate all the required operations of the multimedia system even if these operations may only be needed infrequently. In software such overdimensioning has little consequence but in hardware it increases the complexity of the design and the production cost.

With the emergence of high-performance FPGAs (field programmable gate arrays) [1], we have access to both the required performance and enough flexibility. In the RESUME project (Reconfigurable Embedded Systems for Use in

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