A 250-kHz 94-dB Double-Sampling $\Sigma\Delta$ Modulation A/D Converter With a Modified Noise Transfer Function

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***Abstract*—This paper presents a high-order double-sampling single-loop $\Sigma\Delta$ modulation analog-to-digital (A/D) converter. The important problem of noise folding in double-sampling circuits is solved here at the architectural level by placing one of the zeros in the modulator's noise transfer function at half the sampling frequency instead of in the baseband. The resulting modulator is of fifth order but has the baseband performance of a fourth-order modulator. Through the use of an efficient switched-capacitor implementation, the overall circuit uses only four operational amplifiers and hence, its complexity is similar to that of a fourth-order modulator.**

An experimental 1-bit modulator was designed for an oversampling ratio of 96 and a bandwidth of 250 kHz at a 3.3-V supply in a conservative 0.8-μm standard CMOS process. Due to the double-sampling, the sampling frequency is 48 MHz, although the circuits operate at a clock frequency of only 24 MHz. The circuit achieves a dynamic range of 94 dB. The peak signal-to-noise ratio and signal-to-noise-plus-distortion ratio were measured to be 90 and 86 dB, respectively. The power consumption of the complete circuit including clock drivers and output pad drivers was 43 mW. The analog blocks (opamps, comparators, etc.) consume 30 mW of this total.

***Index Terms*—analog-to-digital conversion, double sampling, sigma-delta modulation.**

I. Introduction

SIGMA-DELTA modulation is a proven technique to realize high- and very high-resolution analog-to-digital converters (ADCs). Where traditional implementations relied on a single-bit quantizer, today the matureness of dynamic element matching techniques allows the use of a multibit quantizer [1]–[4]. This way, several modulator architectures can achieve high performance. For this reason, the performance of an actual $\Sigma\Delta$-modulation A/D conversion circuit is likely to be limited by the circuit performance and not by the performance of the overall modulator architecture. Hence, it is of utmost importance to have a high-performance and efficient circuit-level implementation. This can be achieved by the use of double-sampling techniques. Here, the circuit operates during both clock phases of the master clock. This way, a sampling frequency twice the master-clock frequency is achieved [5]–[16]. Unfortunately, double-sampling $\Sigma\Delta$-modulator ADCs are sensitive to path mismatch, which causes quantization noise to fold from half the sampling frequency back in the signal band. In the past, three solutions for this problem have been proposed. The first uses dynamic element matching techniques to shape the folded noise out of the signal band [9], [10]. The second approach uses a bilinear input integrator [11]–[14]. Finally, an approach based on modifying the noise transfer function was introduced in [15] and [16].

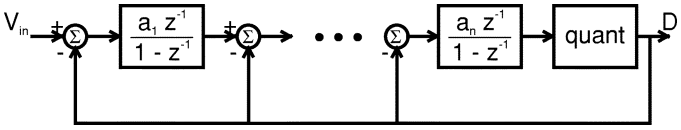

Fig. 1. Typical structure of a $\Sigma\Delta$ modulation ADC.

In this paper, we present a circuit that uses the concept of the modified noise transfer function in a single-loop fifth-order $\Sigma\Delta$ ADC with 250-kHz bandwidth. Here, the noise transfer function has one zero at half the sampling frequency and four zeroes in the baseband. To the best of our knowledge, this is the first reported circuit that implements this concept. The measurements confirm that this technique indeed resolves the problem of noise folding in double-sampling $\Sigma\Delta$ ADCs.

II. Double Sampling and Noise Folding

Fig. 1 shows a diagram of a typical implementation of a switched-capacitor $\Sigma\Delta$ modulator with an input $V_{\rm in}$ and an output D. It consists of a cascade of integrators and a (low-resolution) quantizer. Such a structure implements an A/D conversion where the digital output D is an approximation of the input $V_{\rm in}$. By employing a common white-noise approximation for the quantizer, we can write in the Z-domain

$$D(z) \approx V_{\rm in}(z) + {\rm NTF}(z)\, Q(z) \tag{1}$$

where ${\rm NTF}(z)$ corresponds to the noise transfer function of the modulator and $Q(z)$ to the additive quantization error of the quantizer [17]. The magnitude of the NTF is made small in the signal band by design. Hence, D is a close approximation of the input $V_{\rm in}$ (in the signal band).

The main building block in the structure of Fig. 1 is an integrator. Fig. 2 shows a double-sampling circuit implementation for such an integrator [9]–[16]. It consists of an operational amplifier (opamp), a fixed feedback capacitor $C_{\rm FB}$ and two nominally matched switched input capacitors C_1 and C_2. As is common, the circuit operates on two nonoverlapping clock

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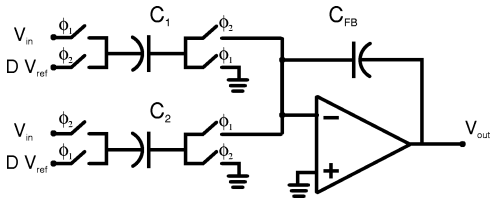

Fig. 2. Basic double-sampling integrator.

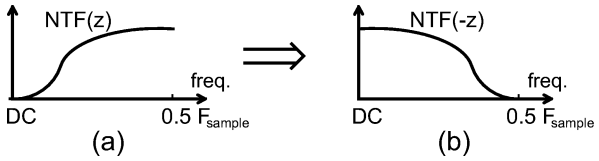

Fig. 3. (a) NTF and (b) folded NTF of a conventional $\Sigma\Delta$ modulator.

phases ϕ_1 and ϕ_2. However, the output voltage $v_{\rm out}$ of the integrator is updated on both clock phases ϕ_1 and ϕ_2 because the two switched input capacitors operate in tandem. Hence, the sampling frequency $F_{\rm sample}$ equals twice the master clock frequency.

Unfortunately, the two input sampling capacitors C_1 and C_2 can only be matched with a limited accuracy. It can be shown that this results in an amplitude modulation (AM) effect of the integrator's input signal with half the sampling frequency [9]–[16]. In the spectral domain, an AM modulation with half the sampling frequency corresponds to a translation of the spectrum from half the sampling frequency to the low-pass baseband (folding). Due to the operation of the overall loop, the major part of the integrator's input signal consists of quantization noise. Hence, path mismatch between the two input sampling capacitors C_1 and C_2 results in quantization noise being folded from half the sampling frequency into the low-pass baseband. More quantitatively, it was shown in [16] that this noise folding results in an additional noise contribution $N_{\rm Fold}$ where

$$N_{\rm Fold}(z) \approx \delta\, Q(-z)\, {\rm NTF}(-z) \tag{2}$$

where δ equals the mismatch between both sampling capacitors: $\delta = (C_1 - C_2)/(C_1 + C_2)$. Notice that the modulation effect corresponds to a substitution $z \rightarrow -z$ in the Z-domain. The occurrence of the additional noise contribution $N_{\rm Fold}$ is called noise folding and is depicted in Fig. 3. In a conventional modulator, NTF$(-z)$ will not be small in the baseband and hence, this additional noise contribution is likely to limit the performance.

Taking inspiration of (2), the effect of noise folding can be tackled by shaping the folded noise out of the low-pass signal band. This is achieved by using an NTF that has one or more zeroes at half the sampling frequency ($z = -1$). This way, the folded noise is greatly reduced in the signal band. This is depicted in Fig. 4.

In practice, one zero at half the sampling frequency should sufficiently suppress the folded noise. By combining this zero with one of the n baseband zeroes, we obtain an NTF(z) of the following form:

$$\text{NTF} = \frac{(z^2-1)(z-1)^{(n-1)}}{P(z)} \tag{3}$$

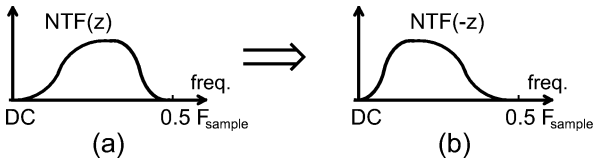

Fig. 4. (a) NTF and (b) folded NTF of a modified $\Sigma\Delta$ modulator.

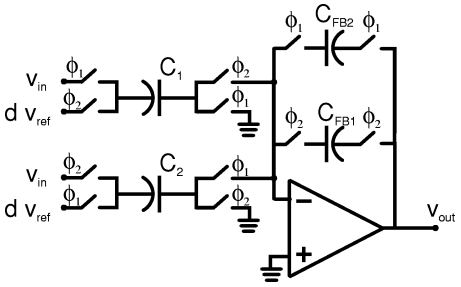

Fig. 5. Double-sampling resonator circuit with a transfer function $\sim z^{-1}/(1-z^{-2})$.

where the denominator $P(z)$ is a polynomial of order $n+1$, and corresponds to the poles of the modulator.

The combination of a baseband zero and a zero at half the sampling frequency can be implemented with a *resonator* structure. In [15] and [16], the double-sampling resonator circuit of Fig. 5 was introduced. This circuit implements a transfer function $\sim z^{-1}/(1-z^{-2})$. By replacing one of the integrators in Fig. 1 with this resonator circuit, we can obtain an NTF of the form of (3).

This work is based on the architecture shown in Fig. 6. Compared with the conventional structure of Fig. 1, in this architecture the last but one integrator is replaced by the resonator of Fig. 5. The resulting modulator requires four opamps but implements a fifth-order noise transfer function. Note that the resonator is placed near the far end of the filter chain. The reason for this is that it introduces additional parasitic (switching) effects due to the additional switched capacitor in the opamp's feedback loop. By placing this resonator near the far end of the filter chain, the equivalent input-referred effect of this is reduced by the gain of the preceding integrators. This way, these effects should be negligible.

III. System-Level Design

One of the first steps in the system level design of a $\Sigma\Delta$ modulator is the choice of the quantizer resolution. From (2) it can be shown that the problem of noise folding can be alleviated substantially by using a multibit quantizer [16]. This way, the overall quantization noise is reduced directly. Hence, the quantization noise that can be folded into the baseband is also reduced. Therefore, a single-bit double-sampling $\Sigma\Delta$ ADC corresponds to the most challenging case. For this reason, we decided to use a single-bit version to demonstrate the strength of the concept of a modified NTF. It is worthwhile to note that in several situations, a single-bit $\Sigma\Delta$ ADC remains the preferable choice in despite of the maturity of multibit $\Sigma\Delta$ modulation [18].

A potential disadvantage of the proposed approach is that the order of the overall modulator is one higher than that of a conventional modulator. In our prototype, for instance, the

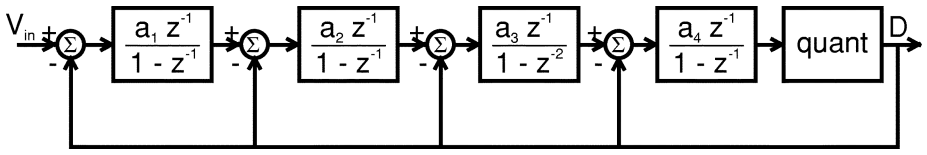

Fig. 6. ΣΔ ADC with a zero at half the sampling frequency, realized by the resonator in the last but one stage.

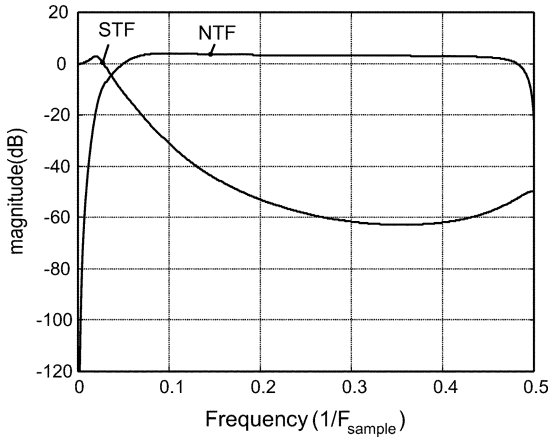

Fig. 7. Magnitude of the signal and noise transfer functions of the modulator structure.

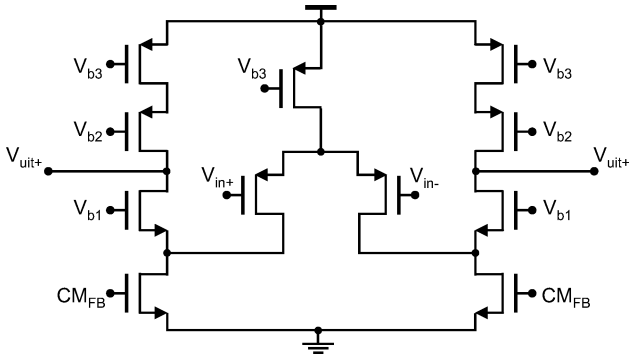

Fig. 8. Folded-cascode OTA used in the double-sampling ADC.

modulator is of fifth order, although its baseband noise-shaping behavior is only of fourth order. This could lead to potential stability problems in a single-bit ΣΔ loop [17]. As demonstrated by the measured results, it is very feasable to keep this additional problem under control.

In a typical systematic design strategy for a ΣΔ modulator, first the NTF is synthesized and then in a second step this NTF is mapped toward a modulator structure [17]. Such a strategy was not feasable here because the modulator structure of Fig. 6 has not enough degrees of freedom to realize an arbitrary NTF: the NTF has five parameters, i.e., the poles of the modulator, but there are only four design parameters, i.e., the value of the four a_i coefficients. Therefore, the modulator was synthesized in an *ad hoc* fashion, i.e., by varying the a_i coefficients until a suitable solution was found. Choosing $(a_1, a_2, a_3, a_4) = (1/10, 1/8, 3/4, 1/2)$ provided a compromise between stability and noise shaping. According to simulation, the modulator was stable for input amplitudes up to 0.75 times the theoretical full scale with these coefficients. At an oversampling ratio of 96, the simulated dynamic range was 108 dB for the ideal modulator. With a realistic path mismatch $\delta = 0.05\%$, this was degraded to 98 dB. The corresponding NTF and signal transfer function (STF) are shown in Fig. 7. From the plot, it is clear that the STF exhibits some peaking with a maximum of $+2.8$ dB around $F_{\rm sample}/50$. The magnitude of the STF crosses the 0-dB line at $F_{\rm sample}/34$. At our oversampling ratio of 96, this peaking effect is still very modest in the signal band (maximum 0.18 dB).

In a final step, the coefficients were scaled to limit the output swing of the integrators. This is a common approach in single-bit ΣΔ modulation ADCs [19].

For comparison purposes, a conventional fourth-order double-sampling modulator was also designed based on the approach of [17]. With the same path mismatch $\delta = 0.05\%$, it achieves a dynamic range of only 77 dB.

IV. Implementation and Measurements

A conservative 0.8-μm CMOS process with two metal and two poly layers was selected for the prototype circuit. The circuits for the modulator structure were designed for a supply voltage of 3.3 V and a signal bandwidth of 250 kHz. At the intended oversampling ratio of 96, this corresponds to a sampling frequency of 48 MHz. However, due to the double-sampling, the clock frequency is only 24 MHz. The integrators and resonators were implemented as the fully differential equivalents of the circuits of Figs. 2 and 5. For the opamps, a well-known folded-cascode operational transconductance amplifier (OTA) was used (Fig. 8). A pMOS input differential pair was chosen because its $1/f$-noise performance is superior in this technology. All the current sources were implemented with relatively long-channel transistors to achieve an adequate dc gain. According to simulation, this dc gain is of the order of 60 dB and the differential output voltage swing ± 2 V. The common-mode feedback signal is injected at node $\rm CM_{FB}$. A double-sampled dynamic circuit is used to sense the output common-mode voltage [20]. The comparator is implemented as a simple latch with a preamplifier.

A microphotograph of the resulting CMOS chip is shown in Fig. 9. The ADC core occupies an area of 1.1 mm^2. The complete chip including bondpads and standard cell pad drivers takes 2.7 mm^2 of silicon area.

The chip was packaged in a simple dual in line package and socketed on a two-layer FR4 testboard. For the measurements reported here, it was driven by dc-coupled commercial ADC driver amplifiers.

It was found that the modulator becomes unstable when the input amplitude is higher than -3 dB of the nominal full scale. This corresponds well to the system-level simulations described in Section III. A typical baseband spectrum after decimation is shown in Fig. 10. Here, the ADC was clocked at 24 MHz and

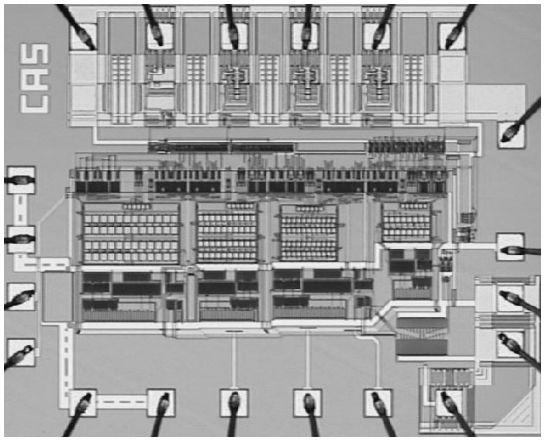

Fig. 9. Chip microphotograph.

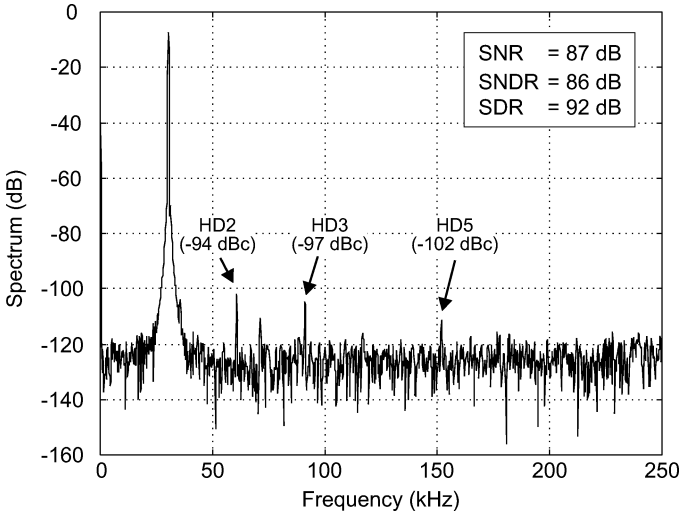

Fig. 10. Baseband spectrum after decimation.

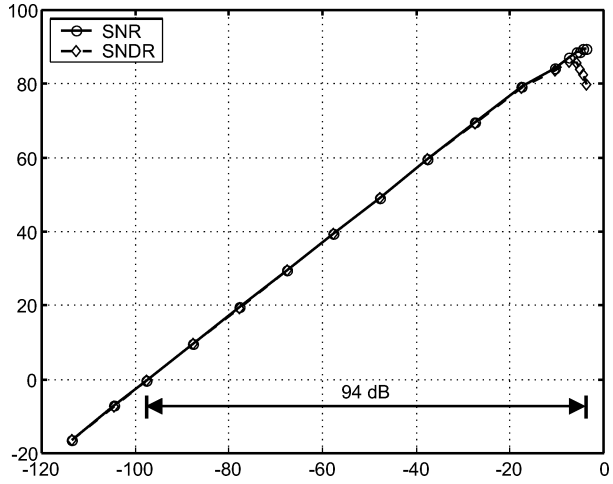

Fig. 11. SNR and SNDR versus input amplitude.

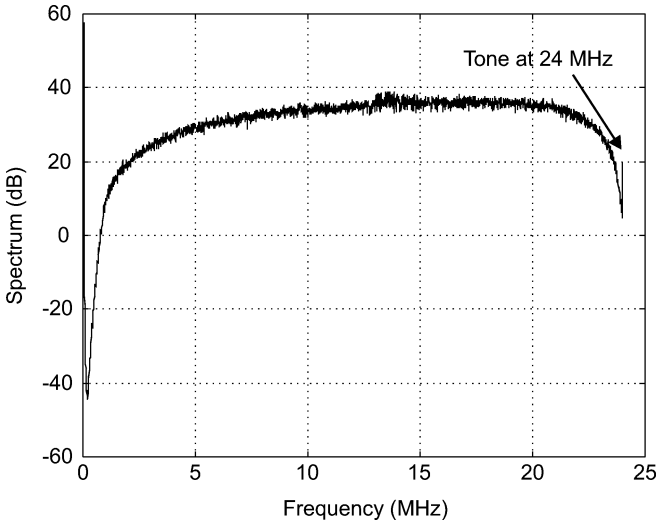

Fig. 12. Output spectrum of the ADC obtained through 31 × spectral averaging of 2^{13}-point windowed FFTs.

driven by a 30-kHz sine-wave input signal with an amplitude of −7.5 dB of the nominal full scale. The signal-to-noise ratio (SNR) was 87 dB and the signal-to-noise-plus-distortion ratio (SNDR) was 86 dB in this case. The signal-to-distortion ratio (SDR) was 92 dB.

Fig. 11 shows the SNR and SNDR versus the input signal level. The plot demonstrates a dynamic range of 94 dB. This is very close to the dynamic range of 98 dB which was predicted by the system level simulation during the architectural design. At high input levels (larger than −6 dB) the distortion (third harmonic) started to increase. This way, the peak SNDR was limited to 86 dB. The peak SNR was 90 dB.

The overall Nyquist-band spectrum for the same −7.5-dB input signal as of Fig. 10 is shown in Fig. 12. To obtain a better view of the noise spectrum, a 31 × spectral averaging of 2^{13}-point windowed fast Fourier transforms (FFTs) was performed. The notch at half the sampling frequency (24 MHz) is clearly visible. The spectrum also exhibits a tone at half the sampling frequency. This tone is attributed to mismatched offsets in the two paths. This could be caused by mismatched signal-independent charge injection in the integrators. Obviously, this tone does not affect the baseband performance in any way.

In a similar way as quantization noise is folded back, input signals near the Nyquist frequency will also fold back to the baseband due to mismatch of the input sampling capacitors. In practical circuits, there is a second mechanism that causes input signal folding, i.e., skew between the edge of both sampling phases ϕ_1 and ϕ_2. This gives a phase-modulation effect of the input signal [21]. To illustrate these phenomena, the $\Sigma\Delta$ modulator was clocked at 24 MHz and driven by a 24.02-MHz input signal with an amplitude of −20 dB of full scale. Here, the same setup as for the measurements of Figs. 10–12 was used except that the on-board anti-aliasing filter was removed. The corresponding baseband spectrum is shown in Fig. 13. Next to an aliased second-harmonic (48.04 MHz), the figure clearly exhibits a folded 20-kHz tone of about −50 dB. This folded tone is nearly entirely generated by skew between ϕ_1 and ϕ_2. As expected, varying the duty cycle of the clock resulted in the amplitude of the folded tone going up and down. This way, the folded tone could be reduced to −80 dB, which is close to a level that could be expected from path mismatch. Although this signal-folding phenomenon does not alter the baseband performance, it is important to note that it gives an additional con-

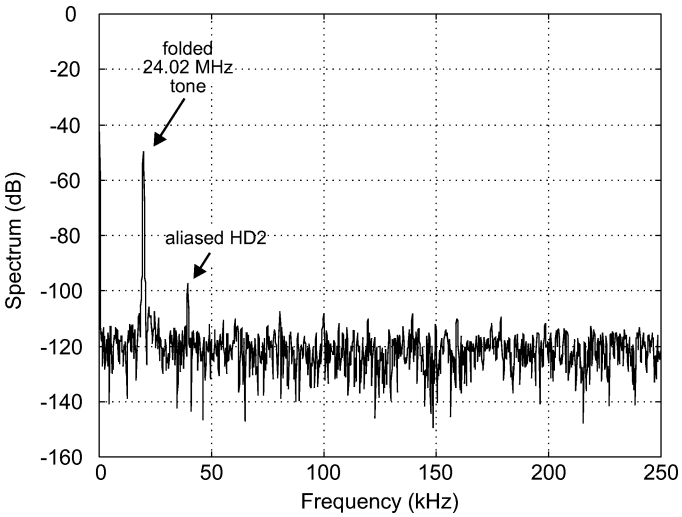

Fig. 13. Baseband spectrum after decimation for a 24.02-MHz input tone.

straint to the anti-aliasing filter which should also suppress input signal folding.

The power consumption in the analog part (opamps, biasing, and comparators) was 30 mW, almost independent of clock or signal frequency. This is due to the fact that all of these analog blocks were designed to operate in class A. A common approach to reduce power consumption in a switched-capacitor ADC is to scale the capacitors (and the opamps) in the second and later integrators [22], [23]. This technique could have been applied here but was not used in this prototype in order to save design time. It is estimated that the power consumption in the analog part could be further reduced by a factor of 2 to 3 by suitable capacitor scaling.

The digital blocks were powered by a separate supply pin and hence, their power consumption was measured separately. This digital circuitry consists of clock drivers and output pad drivers. In this 0.8-μm technology, these circuits consume an additional 13 mW at the 24-MHz clock frequency. According to simulation, the clock drivers consume 5 mW of this and the output pad drivers consume the rest. Note that the decimation filters were not integrated in this circuit. The main performance characteristics of the ADC are summarized in Table I.

TABLE I
PROTOTYPE PERFORMANCE

Technology	0.8μm CMOS (2M2P)
Supply Voltage	3.3 V
Clock Frequency	24 MHz
Bandwidth after decimation	250 kHz
Power consumption	30 mW Analog blocks
	13 mW Clock and pad drivers
Peak SNDR	86 dB
Peak SNR	90 dB
Dynamic range	94 dB
Reference voltage	± 1.5 V
Chip area	2.7 mm^2 (incl pads)
	1.1 mm^2 (excl pads)

V. CONCLUSION

We have presented a fifth-order single-loop double-sampling ΣΔ-modulation ADC. The important problem of noise folding is solved at the architectural level through the use of a modified NTF. Here, one zero is placed at half the sampling frequency and the remaining four zeros are placed in the baseband. Hence, our modulator is of fifth order but has the baseband performance of a fourth-order modulator. Through the use of an efficient switched-capacitor implementation, the overall circuit uses only four operational amplifiers and hence, its complexity is similar to that of a fourth-order modulator.

The experimental 1-bit modulator was designed for an oversampling ratio of 96 and a bandwidth of 250 kHz at a 3.3-V supply in a conservative 0.8-μm standard CMOS process. Due to the double-sampling, the sampling frequency is 48 MHz although the circuits operate at a clock frequency of only 24 MHz. The circuit achieves a dynamic range of 94 dB. The peak SNR was measured to be 90 dB and the peak SNDR was 86 dB. The power consumption of the complete circuit including clock drivers and output pad drivers was 43 mW. The analog blocks (opamps, comparators, etc.) consume 30 mW of this total. This performance compares favorably to other recently published ADCs in the same frequency range [24]–[27].

REFERENCES

[1] R. Schreier and B. Zhang, "Noise-shaped multibit D/A converter employing unit elements," *Electron. Lett.*, vol. 31, no. 20, pp. 1712–1713, Sept. 1995.
[2] L. Hernandez, "A model of mismatch-shaping D/A conversion for linearized DAC architectures," *IEEE Trans. Circuits Syst. I*, vol. 45, pp. 1068–1076, Oct. 1998.
[3] I. Galton, "Spectral shaping of circuit errors in digital-to-analog converters," *IEEE Trans. Circuits Syst. II*, vol. 44, pp. 808–817, Oct. 1997.
[4] P. Rombouts and L. Weyten, "A study of dynamic element matching techniques for 3-level unit elements," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 1177–1187, Nov. 2000.
[5] S. Bazarjani and W. Snelgrove, "A 160-MHz fourth-order double-sampled SC bandpass sigma-delta modulator," *IEEE Trans. Circuits Syst. II*, vol. 45, pp. 547–555, May 1998.
[6] P. Rombouts and L. Weyten, "A CMOS 12-bit 15 Msample/s digitally self-calibrated pipelined A/D converter," in *Proc. Eur. Solid State Circuits Conf.*, Duisburg, Germany, Sept. 1999, pp. 326–329.
[7] U. Moon, "CMOS high-frequency switched-capacitor filters for telecommunication applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 212–220, Feb. 2000.
[8] P. Rombouts, W. De Wilde, and L. Weyten, "A 13.5-bit 1.2 V micropower extended counting A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, pp. 176–183, Feb. 2001.
[9] T. Burmas, K. Dyer, P. Hurst, and S. Lewis, "A second-order double-sampled delta-sigma modulator using additive-error switching," *IEEE J. Solid-State Circuits*, vol. 31, pp. 284–293, Mar. 1996.
[10] C. Thanh, S. Lewis, and P. Hurst, "A second-order double-sampled delta-sigma modulator using individual-level averaging," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1269–1273, Aug. 1997.
[11] H. Yang and E. Elmasry, "Double sampling delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 43, pp. 524–529, July 1996.
[12] D. Senderowicz, G. Nicollini, S. Pernici, A. Nagari, P. Confalonieri, and C. Dallavale, "Low-voltage double-sampled ΣΔ converters," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1907–1919, Dec. 1997.
[13] A. Nagari, A. Mecchia, E. Viani, S. Pernici, P. Confalonieri, and G. Nicollini, "A 2.7-V 11.8-mW baseband ADC with 72-dB dynamic range for GSM applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 798–806, June 2000.

[14] K. Vleugels, S. Rabii, and B. Wooley, "A 2.5-V sigma-delta modulator for broadband communications applications," *IEEE J. Solid-State Circuits*, vol. 36, pp. 1887–1899, Dec. 2001.
[15] P. Rombouts, J. Raman, and L. Weyten, "An efficient technique to eliminate quantization noise folding in double-sampling $\Sigma\Delta$ modulators," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 3, Phoenix, AZ, May 2002, pp. 707–710.
[16] ——, "An approach to tackle quantization noise folding in double-sampling $\Sigma\Delta$ modulation A/D converters," *IEEE Trans. Circuits Syst. II*, vol. 50, pp. 157–163, Apr. 2003.
[17] R. Schreier, "An empirical study of high-order single-bit delta-sigma modulators," *IEEE Trans. Circuits Syst. II*, vol. 40, pp. 461–466, Aug. 1993.
[18] C. Wang, S. Ishizuka, and B. Liu, "A 113-dB DSD audio ADC using a density-modulated dithering scheme," *IEEE J. Solid-State Circuits*, vol. 38, pp. 114–119, Jan. 2003.
[19] D. Ribner, "A comparison of modulator networks for high-order oversampling $\Sigma\Delta$ analog-to-digital converters," *IEEE Trans. Circuits Syst.*, vol. 38, pp. 145–159, Feb. 1991.
[20] D. Senderowicz, S. Dreyer, J. Huggins, C. Rahim, and C. Laber, "A family of differential NMOS analog circuits for a PCM codec filter chip," *IEEE J. Solid-State Circuits*, vol. 17, pp. 1014–1023, Dec. 1982.
[21] M. Gustavsson and N. Tan, "A global passive sampling technique for high-speed switched-capacitor time-interleaved ADCs," *IEEE Trans. Circuits Syst. II*, vol. 47, pp. 821–831, Sept. 2000.
[22] T. Cho and P. Gray, "A 10-bit 20-MS/s 35-mW pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 30, pp. 166–172, Mar. 1995.
[23] S. Rabii and B. Wooley, "A 1.8-V digital-audio sigma-delta modulator in 0.8-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 32, pp. 783–796, June 1997.
[24] P. Maulik, M. Chadha, W. Lee, and P. Crawley, "A 16-bit 250-kHz delta-sigma modulator and decimation filter," *IEEE J. Solid-State Circuits*, vol. 35, pp. 458–467, Apr. 2000.
[25] O. Oliaei, P. Clément, and P. Gorisse, "A 5-mW sigma-delta modulator with 84-db dynamic range for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 37, pp. 2–10, Jan. 2002.
[26] J. Grilo, I. Galton, K. Wang, and R. Montemayor, "A 12-mW ADC delta-sigma modulator with 80 db of dynamic range in a single-chip bluetooth transceiver," *IEEE J. Solid-State Circuits*, vol. 37, pp. 271–278, Mar. 2002.
[27] H. Aboushady, F. Montaudon, F. Paillardet, and M. Louerat, "A 5 mW, 100 kHz bandwidth, current-mode continuous-time $\Sigma\Delta$ modulator with 84 db dynamic range," in *Proc. Eur. Solid State Circuits Conf.*, Florence, Italy, Sept. 2002, pp. 283–286.

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