Toward Fast and Accurate Architecture Exploration in a Hardware/Software Codesign Flow

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Abstract: – Embedded systems design combines software implementations running on an on-chip processor and dedicated hardware components. It also introduces IP-components (Intellectual Property) to be reused and integrated in Systems-on-a-Chip (SoCs). This means a tremendous paradigm shift from the traditional system design. This paper introduces an embedded systems design flow in which the major challenge is the exploration of the design space for optimal architecture configurations. We show that automation of this architecture exploration phase heavily relies on fast and relatively accurate performance estimates for both hardware and software implementations simultaneously. For performance estimation of hardware, we advocate the introduction of a priori interconnect estimations in architecture exploration tools and show how such estimates can be used beneficially.

Key-Words: – Embedded Systems Design, Hardware/Software codesign, A Priori Interconnect Estimation.

1 Introduction

Today, the technological world is no longer dominated by microprocessors. Many systems around us (cellular phones, cars, airplanes, washing machines, etc.) contain and are controlled by electronic chips consisting of both processor blocks to execute software programs and dedicated hardware blocks for the fast evaluation of specific functions. Such systems are called embedded systems. In fact, embedded systems already largely outnumber computer chips. With the progress in technological capabilities (driven by Moore's law, stating that the number of transistors on a chip doubles every 18 months) it is currently possible to combine several components of embedded systems on a single chip. This has become known as System-on-a-Chip (SoC) design.

The design of embedded systems and of SoCs introduces many design challenges. Analogue and RF components are starting to be integrated together with the rest of the system and their design can no longer be seen separate from the overall system design. Another major challenge is the increased freedom to choose the system architecture and tailor it to the application at hand. The number of processing cores available for embedded systems is increasing rapidly and also predesigned hardware blocks (Intellectual Property - IP - blocks) are becoming widely available. Combine this with the choice between either a software implementation on a processor and a hardware approach on a dedicated hardware part (or IP block). The conclusion: an exponential increase in the number of design choices. Within this vast range of choices, the embedded system designer has to optimize for power, timing, area, yield, cost, or other performance criteria.

Evaluating the performance criteria in detail for all possible designs and then picking the best one, is simply impossible. The evaluation of the different architectures has to be based on preliminary, very fast, but reasonably accurate performance estimates. In this paper, we focus on existing techniques for estimating performance parameters of hardware IP blocks based on a priori interconnect prediction. We break a lance for further research in the domain of a priori performance estimates of hardware and software implementations in the embedded systems context. Based on such estimates, automating the exploration of architecture design options becomes feasible and an easier and more automated design flow for embedded systems comes within reach.

Section 2 presents an overview of the embedded systems design flow and shows why very fast performance estimates are crucial in such a flow. Current research on performance estimates in hardware is introduced in section 3.