Design Metholodogy Development for VCSEL-based Guided-Wave Optical Interconnects

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Abstract

In systems with a high density of multi-gigabit per second communication channels—each spanning distances of a few cm to about a metre—optical interconnects are put forward as an alternative to traditional electrical interconnections. The optics should introduce several advantages: higher channel bit rates, denser interconnect and less drive power.

While the technology of VCSELs, photodetectors and different guidewave systems has made much progress over the past decade, the design space of their integration into a full solution has not nearly received the amount of exploration as the individual link building blocks have.

In this paper, we discuss the development of a design methodology for optical interconnects, beginning with a systematic exploration of their design space. To this end, circuit-level simulation models for optical interconnects have been developed that enable prediction of some important system-level properties (such as timing characteristics) of various setups.

Background

Technological development is pushing chip performances higher every day. Feature sizes are decreasing, while chip size and data rates continue to rise. Optimal exploitation of this increasing number of faster devices per chip is often hampered by too slow a communication rate between interconnected integrated circuits [1]. The problem has already become a critical bottleneck in some applications with very intensive data traffic, and is expected to proliferate into more mainstream designs as well in the coming years [2].

In order to satisfy this increasing demand for interconnect bandwidth at the PCB level, optical solutions are being widely investigated, as for electrical interconnects a further throughput increase is fundamentally limited by RLC effects [3]. Not hampered by this limit, photonic links intrinsically provide low-power high-bandwidth interconnect; they do not suffer from electromagnetic interference and have potential to scale with future generations of silicon ICs [1].

The technology of the building blocks of optical interconnects has made immense progress over the past decade. During the past few years, much focus has been put on the use of parallel guided-wave optical interconnects, i.e., transceivers consisting of 2D arrays of VCSELs and photodetectors which are directly flip-chipped onto the processing chip surface, while using waveguide structures for an alignment-tolerant interconnection [4]. Free-space optical interconnects (FSOI) are getting much attention as well. In case of parallel interconnects, the main problem associated with FSOI is that the maximal allowable misalignment between the source and detector arrays is only feasible if the distance between sources and detectors is rather small compared to the source and detector pitch. When this distance becomes relatively large, this leads to a complex mechanical system design. We will therefore only discuss waveguided links here.

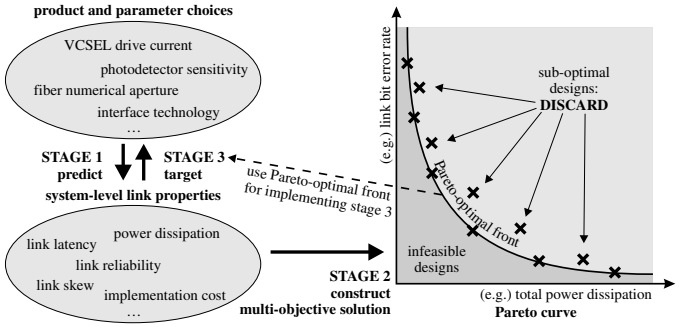

Figure 1: Design methodology development in three stages.

Design Space Exploration

When an optical interconnect system is being conceived for a particular application, the designer gets confronted with a large number of design options concerning optical devices, their integration with CMOS and their driving/receiving circuits, systems for digital encoding and clock recovery, waveguides and connectors and packaging methods yielding optically accessible chips. The choices to be made range from decisions on overall approaches to the fine-tuning of continuously valued parameters, e.g., the numerical aperture of a fiber.

Many choices have a profound impact on system-level properties of the interconnect: feasibility, timing characteristics, reliability and production and operating costs. Exploring the design space and making the right choices is not a simple task, as multiple objectives are to be optimised simultaneously, and the effect of individual choices on the combined system is not easily quantified.

Design Methodology Development

To alleviate the system designers' work, we are currently implementing a systematic way of making these design choices, i.e., constructing a design methodology for parallel guided-wave optical interconnects in an opto-electronic system. The eventual target is to formalise the result of this design methodology development into a design tool. When the designer states some interconnect requirements, this design environment should assist her in making decisions on product and parameter choices. To achieve this goal, we have set up a methodology development program comprising three stages (figure 1):

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1. To begin with, the combined impact of individual link building block variations on the properties of the complete interconnect system is investigated. This comprises the development of tools to predict how system-level link properties will change when certain parameters are adapted.

2. In a second stage, the design space of optical links is searched for setups that yield favourable system-level properties. The Pareto-optimal front is constructed: this is the remaining set of setups after those are discarded that are uniformly worse than others with respect to the system-level properties. Essentially, this front will result in a multi-objective solution for optical links, in such a way that, for each solution, no system-level property can be improved without making some other property worse.

3. In a third stage, using these front data, a design tool is developed that helps a system designer attain the optimal trade-off between system-level properties, after a design-specific specification of boundary conditions and a global cost function for these properties. The tool searches for the system-level properties corresponding to this optimal trade-off and maps them onto a design setup expected to yield these properties. In essence, this is the reverse mapping of what is done in stage 1.

Circuit-level Link Simulation

At this point, the setup for the first stage is being finished. In this stage, time-domain simulation capability of the optical interconnect is necessary to predict global link properties, as some parts of the optical interconnects exhibit a complex internal state, nonlinear behaviour and dynamic interactions triggered by optical, thermal as well as electrical quantities. To this end, circuit-level simulation models for the most important link components have been implemented in the mixed-signal modelling language Verilog-AMS and integrated into a simulation framework [5]. A simulation example is shown in figure 2.

The implementation of these models has not been straightforward. While driver and receiver circuit netlists are directly suitable for simulation, intellectual property protection inhibits their direct distribution. We have therefore implemented behavioural models of the functional subsystems in these circuits instead. Furthermore, a circuit-level multimode VCSEL model is a complex project in its own right. Currently, we are using a mix of the simulation package *VISTAS* by Jungo [6] and the VCSEL model proposed by Mena, et al. [7].

For the VCSEL model and the optical path, the fitting process of model parameters to a real-world setup is complex as well. For the latter, the losses and optical crosstalk are very setup-specific: they heavily depend on the mechanical setup (packaging and connectorisation approach) and the specific waveguide characteristics.

Currently, a demonstrator system is being developed which we can use to verify the accuracy of our method.

Conclusion and Further Work

In this paper, we have outlined the need for a design methodology for optical interconnects and described a methodology development approach. Furthermore, we have discussed circuit-level simulation models to enable the extraction of some system-level properties of different optical interconnect setups.

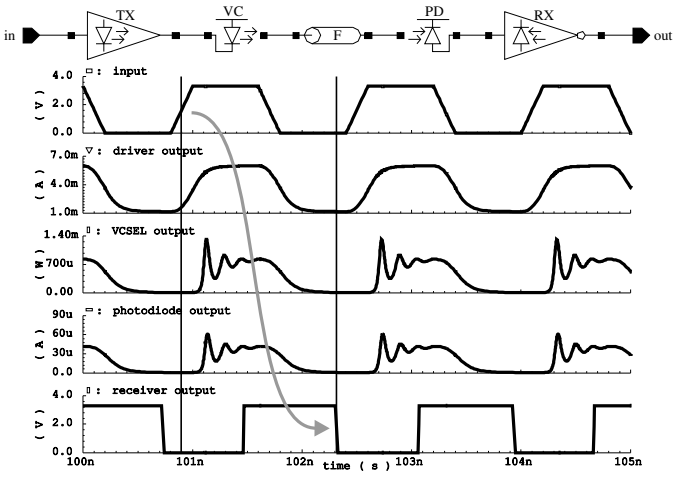

Figure 2: Sample setup of a circuit-level transient simulation of a complete optical interconnection (fictive parameter values).

This research is clearly a work in progress. While we can presently use the implemented models to explore the design space, we will also investigate some important model extensions. Currently, our setup enables the simulation of just the best, typical or worst cases. We would also like to incorporate the statistical nature of some parameters in the models, such as the misalignment of a VCSEL-fiber coupling. A disruptive effect that should additionally be accounted for is the occurrence of substrate noise at the receiver side: a photocurrent of just a few μA is amplified there to normal signal levels. Noise injected into the substrate by switching digital cells could harm the signal integrity in the first amplifier stage. Existing substrate noise modelling tools are currently being evaluated.

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