

A Comparison of Various Terminal-Gate Relationships for Interconnect Prediction in VLSI Circuits

Joni Dambre, Student Member, IEEE, Peter Verplaetse, Dirk Stroobandt, Member, IEEE
and Jan Van Campenhout, Member, IEEE
Ghent University, ELIS Department, Ghent, Belgium
E-mail: {jdambre, pvrplaet, dstro, jvc}@elis.rug.ac.be

Abstract—Over the years different interpretations of Rent's rule and different ways of estimating the Rent parameters have emerged. In general, these parameters are extracted from the average terminal-gate relationship for a set of circuit modules. We show that this relationship (the Rent characteristic) strongly depends on the definition of the circuit modules. These can be generated in many different ways, either from the topology of the circuit graph or, in a geometric way, by cutting regions from a circuit layout. The resulting Rent parameters can be quite far apart. This paper discusses the fundamental differences between the topological and the two geometric interpretations of the Rent characteristic that are expected to be most appropriate for current wirelength estimation techniques. Our discussion is based on experimental data, as well as on a theoretical model that can be used to estimate certain geometric Rent characteristics from the topological Rent parameters. Using this model, we derive a theoretical lower limit to the value of the average geometric Rent exponent. We also study the impact of the placement approach and placement quality on the geometric Rent characteristics.

Keywords—Rent's rule, interconnect complexity, partitioning, placement

I. INTRODUCTION

Landman and Russo's paper [11] is probably the most frequently cited paper in the context of circuit interconnect prediction, targeting important properties such as wirelength distribution and average wirelength. These authors used a hierarchical partitioning of a circuit into modules, so as to obtain a good placement leading to low wirelengths. This partitioning minimizes the module terminal count, as well as the maximal module size. For the resulting partitionings, they plotted the average terminal count versus the average module size, and found a relationship that could be approximated by a power law

$$T = tG^p, \quad (1)$$

where T is the number of terminals required to connect a module to the remainder of the circuit and G is the number of gates in that module. They called this power law Rent's rule and the coefficient t and exponent p are now generally referred to as the Rent coefficient and the Rent exponent, respectively.

However, as Landman and Russo described, the relationship between the average module size and the module pin count is more complex than the simple power law expressed by Rent's rule. Indeed, it usually applies only to module sizes well below the overall circuit size (Figure 1). The range of module sizes for which Equation (1) is a good approximation is called region I.

Dirk Stroobandt is Postdoctoral Fellow with the Fund for Scientific Research (F.W.O.)—Flanders

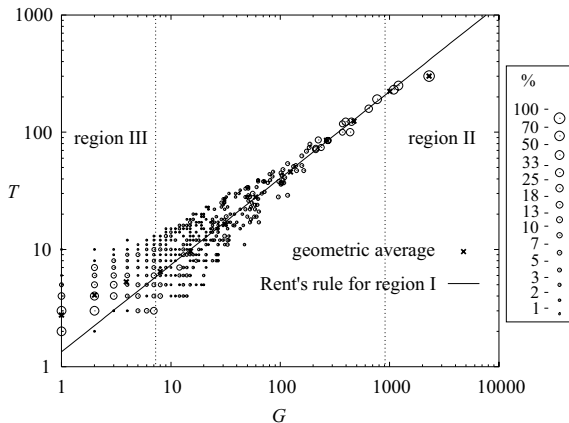


Fig. 1. Typical example of the terminal-gate relationship for a hierarchical bi-partitioning of a circuit (ISCAS85 benchmark 'c5315nr'), showing geometric average values of T vs. G and the optimal, region I power-law fit.

Landman and Russo proposed an expression to model the region corresponding to large module sizes and referred to it as region II.

Since then, other researchers have studied the terminal-gate relationship of circuit modules. A third region, corresponding to small module sizes, was identified [14], [15] and other analytical models were proposed [3]. For some circuits, there hardly remains a region between regions II and III where Rent's rule applies. Therefore, as is done in [18], we will mainly consider the entire terminal-gate relationship or the Rent characteristic

$$T = R(G). \quad (2)$$

In this paper, we make a comparison of various techniques that are currently used to derive terminal-gate relationships. We show that, for a given circuit, indeed many different Rent characteristics exist. These can be purely topological (based only on the circuit graph) or geometric (based on a circuit layout). Hence, the notion of a Rent characteristic only makes sense in combination with the way in which it was obtained. We identify one topological and two geometric Rent characteristics that promise to be appropriate for current wirelength estimation techniques. Based on both a theoretical framework and experimental results, we will offer new insights on these characteristics. In particular, we will show that average geometric

The remainder of this paper is not included as this paper is copyrighted material. If you wish to obtain an electronic version of this paper, please send an email to bib@elis.ugent.be with a request for publication P103.024.pdf.
