# Guided-wave optical interconnects: design methodology development

Research Abstract for Michiel De Wilde <michiel.dewilde@rug.ac.be>
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## 1 Introduction

Technological development is pushing chip performances higher every day. Feature sizes are decreasing, while chip size and data rates continue to rise. Optimal exploitation of this increasing number of faster devices per chip is often hampered by too slow a communication rate between interconnected integrated circuits [3]. The problem has already become a critical bottleneck in some applications with very intensive data traffic, and is expected to proliferate into more mainstream designs as well in the coming years [5].

In order to satisfy this increasing demand for interconnect bandwidth at the PCB level, optical solutions are being widely investigated, as for electrical interconnects a further throughput increase is fundamentally limited by RLC effects [4]. Not hampered by this limit, photonic links intrinsically provide low-power high-bandwidth interconnect; they do not suffer from electromagnetical interference and have potential to scale with future generations of silicon IC's [3].

The technology of the building blocks of optical interconnects has made immense progress over the past decade. During the past few years, much focus has been put on the use of parallel guided-wave optical interconnects, i.e., transceivers consisting of 2D arrays of VCSELs and photodetectors which are directly flip-chipped onto the processing chip surface, while using waveguide structures for an alignment-tolerant interconnection [2, 6].

## 2 Design space exploration

When an optical interconnect system is being conceived for a particular application, the designer gets confronted with a large number of design options concerning optical devices, their integration with CMOS and their driving/receiving circuits, systems for digital encoding and clock recovery, waveguides and connectors and packaging methods yielding optically accessible chips. The choices to be made range from decisions on overall approaches to the fine-tuning of continuously-valued parameters, e.g., the numerical aperture of a fiber.

Many choices have a profound impact on system-level properties of the interconnect: feasibility, timing characteristics, reliability and production and operating costs. Exploring the design space and making the right choices is not a simple task, as multiple objectives are to be optimised simultaneously, and the effect of individual choices on the combined system is not easily quantified.

## 3 Design methodology development

The target of this research is to find a systematic way of making these design choices, i.e., to construct a design methodology for parallel guided-wave optical interconnects in an opto-electronic system. The eventual target is to formalise the result of this design methodology development into a design tool. When the designer states some interconnect requirements, this design environment should assist her in making decisions on product and parameter choices. To achieve this goal, we have set up a methodology development program comprising three stages:

1. To begin with, the combined impact of individual link building block variations on the properties of the complete interconnect system is investigated. This comprises the development of tools to predict how system-level link properties will change when certain parameters are adapted.

2. In a second stage, the design space of optical links is searched for setups that yield favourable system-level properties. The Pareto-optimal front is constructed: this is the remaining set of setups after those are discarded that are uniformly worse than others with respect to the system-level properties. Essentially, this front will result in a multi-objective solution for optical links, in such a way that, for each solution, no system-level property can be improved without making some other property worse.

3. In a third stage, using these front data, a design tool is developed that helps the system designer attain the optimal tradeoff between system-level properties, after a design-specific specification of boundary conditions and a global cost function for these properties. The tool searches for the system-level properties corresponding to this optimal tradeoff and maps them onto a design setup which is expected to yield these properties. In essence, this is the reverse mapping of what is done in stage 1.

## 4 Research status

At this point, the first stage is being worked on. In this stage, time-domain simulation capability of the optical interconnect is necessary to predict global link properties, as some parts of the optical interconnects exhibit a complex internal state, nonlinear behaviour and dynamic interactions triggered by optical, thermal as well as electrical quantities. To this end, circuit-level simulation models for the most important link components have been implemented in the mixed-signal modelling language Verilog-AMS and integrated into a simulation framework [1].

## References

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