MG5
15:15 – 15:30

Demonstration of manufacturable free-space modules for multi-channel intra-chip optical interconnects.

Christof Debaes[a], Michael Vervaeke[a], Heidi Ottevaere[a], Wim Meeus[b], Patrik Tuteleers[a], Marnik Brunfaut[b], Valérie Baukens[a], Jan Van Campenhout[b], Hugo Thienpont[a]
[a]Vrije Universiteit Brussel (VUB), Dep. of Applied Physics and Photonics (TONA/TW), Pleinlaan 2, B-1050 Brussel
[b]Universiteit Gent (RUG), Dep. of Electronics and Information Systems (ELIS), Sint Pietersnieuwstraat 41, B-9000 Gent

Abstract
We investigate the combination of a replicated plastic optical micro-component with an opto-electronic field programmable gate array for multi-channel intra-chip interconnects. Multichannel operation at 10 Mbit/s per channel has been demonstrated.

Introduction
As the current technology of digital systems is progressing, with the further miniaturization of the gate dimensions and the increase of clock speeds, the electronic interconnection technology is not advancing accordingly. Not only is the increased wire resistance, residual wire capacitance, transmission line effects and the increasing inter-wire cross-talk slowing the pace of the interconnect performance evolution. Also an aspect ratio is limiting the maximum bit-rate for conventional electrical interconnects[1]. This aspect ratio limits the maximum information bandwith of a certain wire cross-section. Simply scaling the dimensions of the interconnection is not a solution either for the bandwidth-problem. We therefore choose photons as the physical carrier for the information since they are not limited by an aspect ratio dependend bit-rate.
Many studies have been dedicated to the use of optics to increase the performance of interconnections. A lot of effort over the recent years has been put in determining the potentialities and limitations of optical interconnects since the introduction of optics as a 'wire replacing technology' [2]. While it is still debatable whether on-chip optical interconnects can be advantageous, a recent paper suggests that on-chip interconnect could be beneficial because of the lower latency for comparable dissipated powers, even at subcentimeter length [3].
In this paper we investigate the use of a free-space micro-optical interconnection module to establish an intra-chip interconnection on an opto-electronic field programmable gate array (OE-FPGA) [4]. We work towards a manufacturable solution combining replication techniques and in-house deep lithography with protons (DLP) [5,6]. The proof of manufacturability consists of an investigation on the influence of misalignments and fabrication errors. We also report on our recent link experiments with different free-space optical modules on the OE-FPGA.

The micro-optical pathway block
Heterogeneous integration techniques allow the incorporation of optical components with high-performance CMOS-chips. Different technologies exist to set up the optical link between the devices. One approach consists of using free-space, either by using macro-optics, planar optics or micro-optics. In our approach beams generated by flip-chipped VCSEL arrays are shaped and directed in such a way that efficient and cross-talk free communication links are made possible.

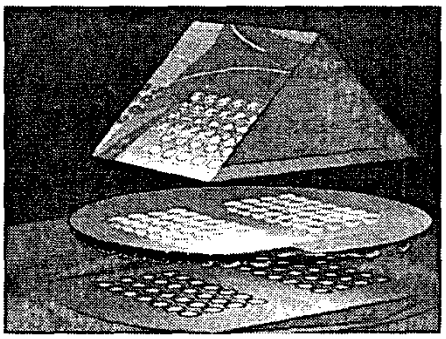

Figure 1: The concept of the 3D micro-optical pathway block.

We use a micro-optical pathway block consisting of micro-lenses and micro-prisms [5] to shape, direct and focus the beams of light from the emitters to the designated detectors. A micro-lens array collects and collimates the light to the micro-mirrors of the prism, which in their turn redirect the beams over 180°. A second micro-lens array receives the redirected beams and focusses onto the detectors (see Fig. 1). With this approach we deliver signals from emitters to detectors over on-chip distances from 750 μm to 4.250 mm. The pathway length between the emitter and detector is kept constant at 8 mm, resulting in a constant latency for the different links, independent of the on-chip interconnect length.
The optical pathway block was designed and fabricated using in-house technology. We use DLP to make optical surfaces, alignment features and lenslet arrays on a single substrate of poly-methyl metacrylate (PMMA). Using alignment holes we are able to glue micro-prisms on the lenslet arrays, resulting in an optical pathway block with 2x8 channels (per micro-prism), consisting of 200 μm diameter lenses on a pitch of 250 μm. Here the number of

channels is limited by our current DLP technique because the prism thickness cannot exceed 500 µm. Another approach we investigated is the use of commercially available glass micro-prisms, enabling us –because of their larger geometrical dimensions- to increase the amount of interconnections per prism. Furthermore, with the reduction of the lensdiameter to 120 µm, we prove that downscaling is an asset of the free-space approach.

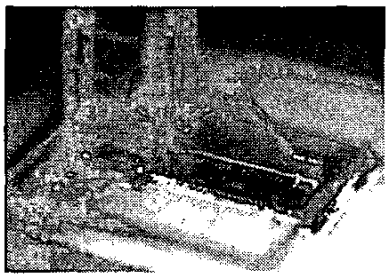

Figure 2: The replicated OPB on the OE-FPGA chip.

DLP is a high precision prototyping technique, but is not suited for low-cost mass-production. We used vacuumcasting [6] to replicate the prototypes of the optical pathway block. The result is a monolithic block (see Fig. 2), consisting of micro-lens arrays, prisms and other features.

Extensive research was conducted to determine the design guidlines for the optical pathway block, along with the necessary tolerances on different design parameters to assess the manufacturability of our concept. With commerial optical design software we showed that transfer efficiencies of 96% and cross-talk levels below –25 dB were attainable with our 200 µm diameter lens system. The result is a system with reasonable tolerances on fabrication and assembly errors allowing for mass-fabrication. The downscaled system with 120 µm lenses is collecting less light (60%) but it shows similar tolerancing values. Cross-talk values below –25 dB are still possible, which indicates that interconnections with this optical pathway block are possible with the cross-talk sensitive OE-FPGA.

Early experiments of multi-channel free-space intra-chip interconnections

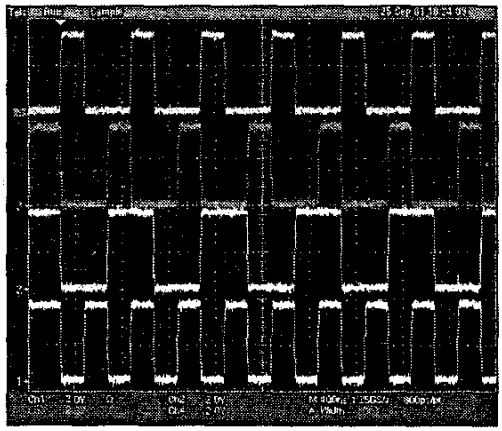

Figure 3: Traces of 4 channels.

Combining our optical pathway block with the OE-FPGA, we demonstrated for the first time to our knowledge a multi-channel intra-chip optical interconnection. The FPGA was programmed to provide four signals on neighboring channels (Fig. 3). Carefull alignment – the lateral alignment tolerance is 4 µm, the working distance requires an accuracy of 35 µm - yielded four perfectly working channels at 10 MB/s with no apparent cross-talk (Fig. 3). We encountered similar tolerancing values and cross-talk behavior as predicted in the study. The poor specifications of the used optical pathway block and the stringent alignment tolerances restricted the communication to 4 simultaneous channels. Furthermore, the chiptester limited the speed to 10 Mbit/s.

At the conference we will present the results with our most recent optical pathway block using the DLP-prisms and full 3D prisms, ensuring a higher number of interconnected channels (64 channels maximum) at the maximal OE-FPGA speed of 80 Mbit/s per channel.

References

[1] H. M. Özaktas and D. A. B. Miller, "Limit to the Bit-Rate Capacity of Electrical Interconnects from the Aspect Ratio of the System Architecture", *J. Parallel and Distributed Computing*, Vol. **41**, pp. 42-52, 1997.

[2] J. W. Goodman, F. J. Leonberger, S.-Y. Kung and R. A. Athale, "Optical interconnections for VLSI systems", *Proceedings of the IEEE*, Vol. **72**, pp. 850-866, 1984.

[3] http://www.intec.rug.ac.be/oiic/index.htm

[4] H. Thienpont, C. Debaes, V. Baukens, H. Ottevaere, P. Vynck, P. Tuteleleers, G. Verschaffelt, B. Volckaerts, A. Hermanne and M. Hanney, "Plastic Microoptical Interconnection Modules for Parallel Free-space Inter- and Intra-MCM Data Communication", *Proceedings of the IEEE*, Vol. **88**, No. 6, (June 2000), pp. 769-779.

[5] B. Volckaerts, H. Ottevaere, P. Vynck, C. Debaes, P. Tuteleers, A. Hermanne, I. Veretennicoff and H. Thienpont, "Deep lithography with protons: a generic fabrication technology for refractive micro-optical components and modules", Asian Journal of Physics, Vol. **10**, No. 2, pp. 195-214, 2001, invited paper.

[6] P. Tuteleers , P. Vynck, B. Volckaerts, H. Ottevaere, V. Baukens, C. Debaes, A. Hermanne, I. Veretennicoff and H. Thienpont, "Replication of refractive micro opto-mechanical components made with Deep lithography with protons", *Symposium on Design, Test, Integration and Packaging om MEMS/MOEMS* (DTIP2001), Cannes, France, Apr. 2001, pp. 329-337.