A Pipelined D/A converter with an improved driving scheme for DMT-signals

P. Rombouts, L. Weyten, W. De Wilde
ELIS-CAS group at Ghent University,
St.-Pietersnieustraat 41, 9000 Gent,
Belgium

Abstract

This paper presents the design of a pipelined switched-capacitor D/A-converter with a novel driving scheme. This driving scheme is optimized for signals with a high crest factor. Such signals occur in modern communication systems such as DMT-based VDSL. The 0.6 μm CMOS prototype circuit was tested with DMT test signals and achieves 12 effective bits for clock frequencies upto 17.664 MHz. The power consumption of the DAC itself is only 60 mW and an additional 25 mW is consumed by a Track&Hold.

1. Introduction

Advanced communication applications such as VDSL require both a high speed and a relatively high accuracy (about 12 effective bits). Today these high-speed D/A-converters are often based on current-steering [1]. In this work an alternative approach is investigated based on pipelined switched-capacitor techniques. Here 10-bit accuracy can easily be obtained due to the inherent good matching properties of integrated capacitors. To enhance the resolution by 2 more bits a novel driving scheme for DMT-signals is applied. This driving scheme exploits the high crest-factor of such a DMT-signal. As a result small input signal values occur much more often than large input values. Based on this property an optimized driving scheme is used. As will be shown later on, this driving scheme improves the linearity for small input signals.

The rest of the paper is organized as follows: in section 2 the pipelined D/A-conversion technique is reviewed, section 3 introduces the RSD-driving scheme, section 4 describes a prototype chip with some experimental results in section 5.

2. Pipelined DAC

2.1. 2-C DAC

Probably the simplest circuit that can be used for D/A-conversion is Suarez' 2-capacitor circuit [2]. It requires only 2 switched capacitors and a few gates to drive the switches. Unfortunately its speed is limited because the circuit is used in a sequential manner to convert the bits one after another. To remediate this a pipelined version

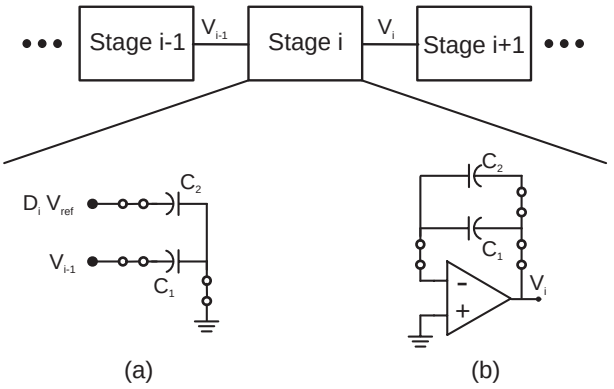

Figure 1. 2-C switched capacitor pipeline DAC-stage with its two-phase operation

was presented [3]. Previous implementations have used a completely passive version of this circuit [4]. Although beneficial in terms of power consumption and speed, the completely passive approach turns out to be sensitive to parasitic effects, which complicates the design. Therefore here an active version was considered, inspired on the variant described in [5]. This pipeline consists of a number of stages that are placed one behind another (see fig. 1). Each stage consists of an operational amplifier and two switched capacitors C_1 and C_2, that are nominally matched. It operates in two phases. During the first 'sampling' phase one of the capacitors is switched to the stages' input to sample the input voltage V_{i-1} while the other one is switched to plus or minus the reference voltage V_{ref} depending on the value of the corresponding bit b_i. In the second 'redistribution' phase the two capacitors are switched in the opamp's feedback loop to generate the stage's output voltage V_i. If both capacitors are perfectly matched this can be described as:

$$V_i = \frac{1}{2}(V_{i-1} + D_i V_{ref}). \quad (1)$$

Here the local code D_i equals -1 if the corresponding bit $b_i = 0$ and $D_i = 1$ if $b_i = 1$. For m stages this leads to:

$$V_m = \sum_{i=1}^{m} 2^{i-m-1} D_i V_{ref}. \quad (2)$$

This corresponds to the desired DAC output voltage.

It should be noted that an actual circuit implementation should be differential although the circuit is drawn single-ended for simplicity.

2.2. N-C DAC

Inspired on McCreary's circuit [6] the pipeline of fig. 1 can be generalized to convert more than 1 bit per stage. Here either unit elements or binary weighted elements can be used. If N unit elements or used the circuit of fig. 2 results where the capacitors $C_1 \ldots C_N$ are nominally matched.

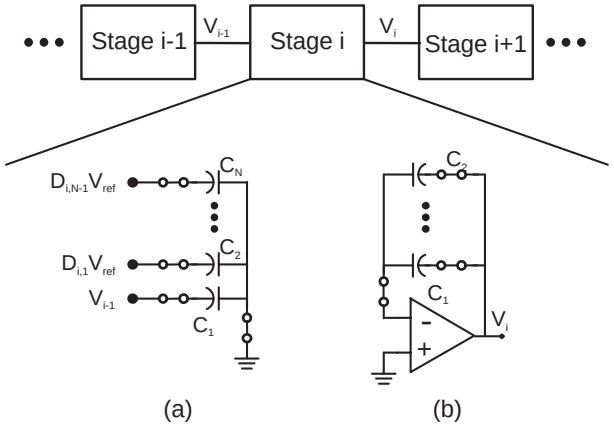

Figure 2. Generalized N-C switched capacitor pipeline DAC-stage with its two-phase operation

Assuming the N capacitors are perfectly matched, the stage's output voltage V_i can again be obtained from its input voltage V_{i-1} and the local codes $D_{i,j}$:

$$V_i = \frac{1}{N}(V_{i-1} + \sum_k D_{i,k} V_{ref}). \qquad (3)$$

In a typical application N would be an integer power of 2. This way the stage still converts an integer number of bits.

2.3. Combination with Nicollini's S&H

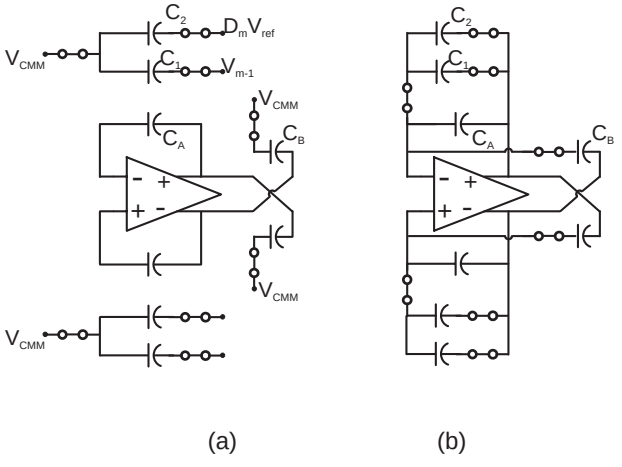

Figure 3. 2-C stage combined with Nicollini's S&H

A drawback of the circuits of fig. 1 and fig. 2 is that their output voltage is only valid during 1 of both clock phases. To overcome this problem the last stage can be integrated into Nicollini's sample & hold circuit [7]. This is shown on fig. 3 for the case of a 2-C DAC-stage. The operation is nearly identical to the normal operation of Nicollini's circuit. During the first phase the input voltage V_{m-1} is sampled on the capacitor C_1 while C_2 is switched to plus or minus V_{ref} according to the value of the code D_m. In the second phase C_1 and C_2 are switched parallel to the capacitor C_A in the feedback loop of the opamp to generate the updated value of the output voltage V_m. At the same time a positive feedback path is generated through the capacitor C_B to cancel the previous charge on the capacitor C_A [7]. For complete cancellation the capacitors C_A and C_B should be matched. Assuming C_1 and C_2 are perfectly matched the resulting output voltage V_m becomes:

$$V_m = \frac{1}{2}(V_{m-1} + D_m V_{ref}). \qquad (4)$$

This exactly performs the same operation of the simple 2-C circuit of fig. 1. Obviously the approach can be combined as well with the generalized N-C technique of fig. 2.

3. RSD Driving scheme

Essentially the structure of fig. 1 gives rise to a binary weight coding. The main problem with such a scheme is that the major carry transition occurs just in the middle of the signal range. For this reason circuit imperfections such as mismatched capacitors will cause large non-linearity errors (INL) exactly here. Unfortunately exactly these input values occur often with DMT input sequences. This is illustrated on fig. 4 where a simulation result for the INL is shown for the circuit of fig 1 in the presence of capacitor mismatch ($\sigma = 0.1\%$)

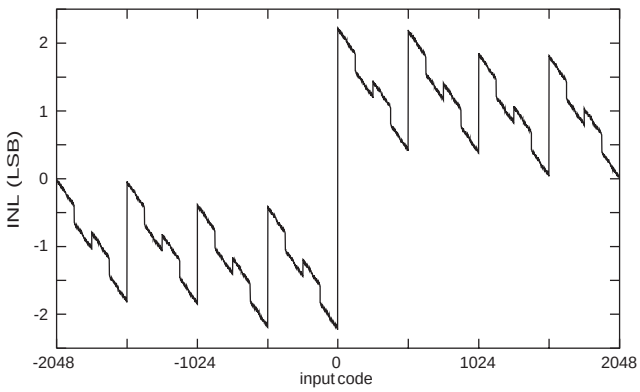

Figure 4. Simulated INL due to capacitor mismatch for the conventional pipelined 12-bit DAC of fig. 1

To overcome this drawback the major carry transitions are shifted away from the middle of the signal range. To achieve this a redundant state is introduced for each stage in the circuit of fig. 1: now the local code D_i can equal

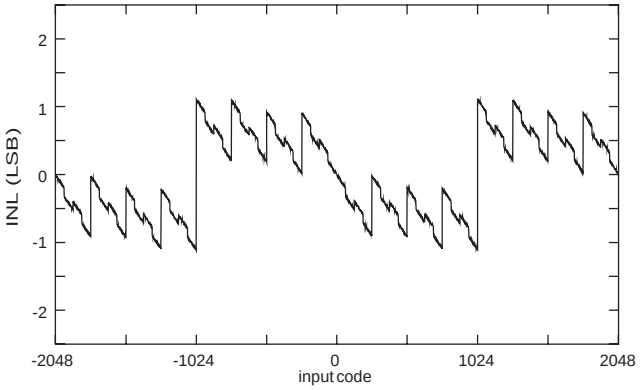

Figure 5. Simulated INL due to capacitor mismatch for the 12-bit DAC with an RSD driving scheme

$-1; 0$ or 1. Depending on the value of D_i the capacitor C_2 is now switched to plus or minus V_{ref} or to common. Hence equations (1) and (2) still remain valid and thus the circuit still operates as a DAC. However since the state $D_i = 0$ is redundant extra freedom is introduced. This is exploited here to shift the major carry transitions as far away as possible from the mid-signal range. It turns out that this is achieved by computing the local codes according to the RSD-algorithm, that is widely used today in cyclic and pipelined A/D-converters [8, 9]. A simulation result for this case is shown on fig. 5. By comparing fig. 4 and 5 it is clear that the linearity at the middle of the input range is improved considerably.

From simulations also the performance for DMT-input signals can be estimated. Such a signal consists of several transmit-bands that are filled with random phase sinewaves that are equally spaced in frequency. The ratio between the signal tones and the spurious tones in the nominally empty bands are a measure for the distortion (Missing Band Depth or MBD) [1]. Simulations for the VDSL frequency allocation scheme indicate that the MBD is improved by as much as 13 dB (2 bits !). This way 12 effective bits can be achieved with only 0.1% capacitor matching.

It should be noted that similar RSD-inspired driving schemes can be conceived for the N capacitor circuits of fig. 2 as well. It is also clear that application of these techniques is not limited to the switched-capacitor, pipelined structures that are described here.

4. CMOS prototype

To demonstrate the effectiveness of the proposed techniques a prototype circuit was designed in a standard 0.6 μm CMOS process for a 3.3 V suppy voltage. The pipeline consists of 7 identical 4-C stages ($N = 4$ in fig. 2). These are followed by a last 2-C stage built around Nicollini's Sample&Hold according to fig. 3 For the 4-C stages, Cho's very power-efficient cascode opamp with low-gain pre-amplifier was used [10]. The *Nicollini* stage must be able to drive resistive loads and therefore here a less efficient two-stage opamp is used. As a result this final stage drains as much power as all the other stages in the pipeline together.

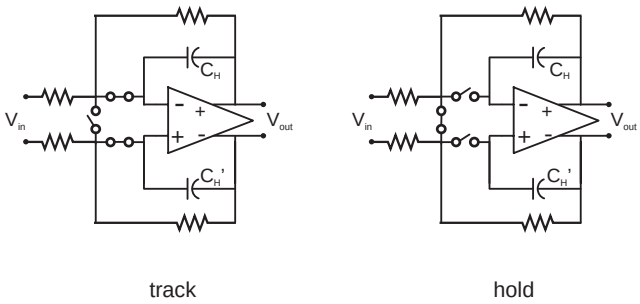

Figure 6. Additional Track&Hold amplifier for linear settling.

An important requirement for the output Sample&Hold amplifier is that its entire transient response must be linear. Although Nicollini's circuit already implements a Sample&Hold function, it was found during design that its transient response is (by far) not linear enough. Therefore an additional more linear Track&Hold amplifier is added. It is based on a simple resistive inverting opamp circuit (see fig. 6). This circuit provides excellent linear settling performance. Moreover it can be used even at an extremely low supply voltage [11]. A drawback is that it increases the power consumption and the noise. Again a two-stage opamp is used here.

A microscope photograph of the complete chip is shown on fig. 7. The total chip area including the bonding pads is 3.1×1.9 mm^2

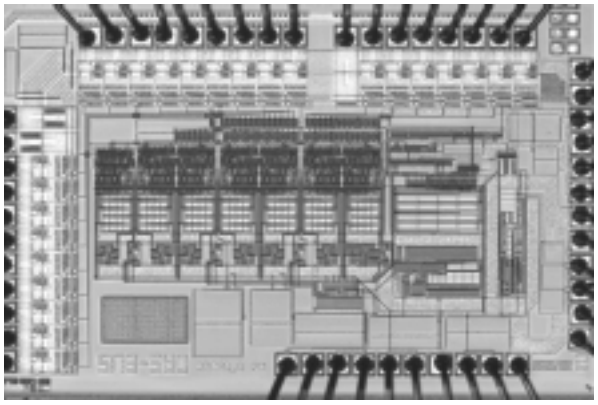

Figure 7. Chip microscope photograph.

5. Experimental results

The circuit was tested by applying VDSL test-sequences to the DAC [1]. The crest-factor was 5.6. The differential DAC output voltage is buffered of chip and applied to a spectrum analyzer. A typical measured result is shown on fig. 8.

As outlined above an important measure for the performance of the DAC is the ratio between the signal tones and

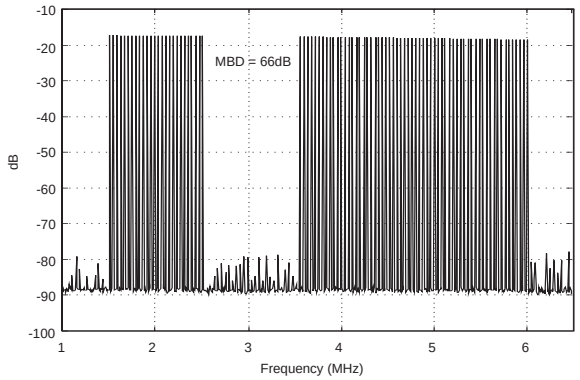

Figure 8. Measured DAC output-spectrum ($f_{clk} = 17.664$ MHz)

the spurious tones in the nominally empty bands (Missing Band Depth or MBD) [1]. From measurements such as that shown on fig. 8 this MBD can be determined. Fig. 9 shows the measured MBD versus the clock frequency. Here it should be noted that the current measurement setup limits the DAC clock frequency to sub-harmonics of the VDSL clock frequency of 35.328 MHz. The DAC could also be configured to work in a test mode where the novel RSD driving scheme is not employed. The results for this case are shown on fig. 9 as well. For the case of RSD driving the circuit achieves an MBD=67 dB for low clock frequencies. This corresponds to 12 effective bits. This performance remains nearly unaffected for clock frequencies upto 17.664 MHz. For the clock frequency of 35.328 MHz the performance is reduced to 9.9 effective bits. In the case of conventional driving an MBD=63 dB is achieved for low clock frequencies. Hence the differenc with the RSD-driving scheme is 4 dB here. For higher clock frequencies the difference with the RSD-case becomes even larger. This confirms that the RSD-driving scheme effectively boosts the performance.

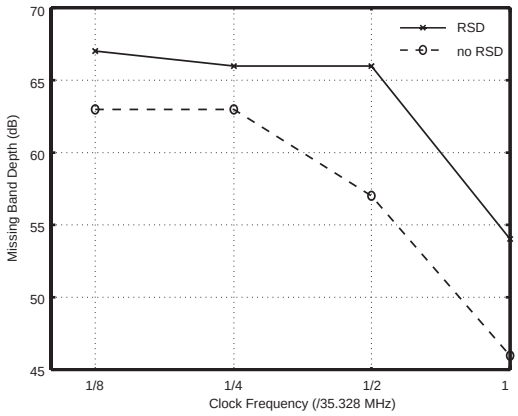

Figure 9. Measured MBD vs. clock-frequency with RSD-coding (bold line) and conventional coding (dashed line)

Clocked at 35.328 MHz, the measured differential output noise was 34 nV/$\sqrt{Hz}$, nearly flat over the entire Nyquist band. With a full-scale differential output voltage range of ± 1 Volt, this corresponds to 0.3 lsb RMS@12bit. The DAC-circuit itself consumes only 60 mW and the Track&Hold (fig. 6) consumes an additional 25 mW.

6. Conclusion

We have presented a switched capacitor DAC that is based on a generalized 2-C principle. High-speed operation is achieved through the use of a pipeline. In addition we have introduced a novel driving scheme that is particularly suitable for DMT-signals with a high crest factor. Such signals occur in modern communication systems such as VDSL. The 0.6 μm CMOS prototype circuit was tested with DMT test signals and achieves 66 dB MBD for clock frequencies upto 17.664 MHz. This corresponds to 12 effective bits. The power consumption of the DAC itself is only 60 mW and an additional 25 mW is consumed by the Track&Hold.

[1] W. De Wilde et al., "Analog Front End for DMT-based VDSL," ISSCC Dig. Tech. Papers, Feb 2002, pp. 328-329.

[2] R. Suarez, P. Gray and D. Hodges., "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques - Part II" IEEE J. Solid-State Circuits, vol. SC-10, No. 6, pp. 379-385, Dec. 1975.

[3] F.-J. Wang, G. Temes and S. Law, "A Quasi-Passive CMOS Pipeline D/A Converter" IEEE J. Solid-State Circuits, vol. 24, No. 6, pp. 1752-1755, Dec. 1989.

[4] A. Rofougaran et al., "A Single-Chip 900-MHz Spread-Spectrum Wirelesess transceiver in 1μm CMOS Part I: Architecture and Transmitter design," IEEE J. Solid-State Circuits, vol. 33, No. 4, pp. 515-534, Apr. 1998.

[5] H. Matsumoto and K. Watanabe., "Switched Capacitor Algorithmic Digital-to-Analog Converters." IEEE Trans. Circuits Syst., vol. CAS-33, No. 7, pp. 721-724, july 1986.

[6] J. L. McCreary and P. R. Gray, "All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques - Part I" IEEE J. Solid-State Circuits, vol. SC-10, No. 6, pp. 371-379, Dec. 1975.

[7] G. Nicollini, P. Confalonieri and D. Senderowicz, "A Fully Differential Sample-and-Hold Circuit for High-Speed Applications," IEEE J. Solid-State Circuits, vol. 24, No. 5, pp. 1461-1465, Oct. 1989.

[8] Bernard Ginetti, Paul G. A. Jespers, André Vandemeulebroecke, "A CMOS 13-b Cyclic A/D Convertor," IEEE J. of Solid State Circuits, vol. 27, No. 7, July 1992, pp. 957-964.

[9] S. H. Lewis, H. S. Fetterman, G. F. Gross, R. Ramachandran and T. R. Viswanathan, "A 10-b 20-Msample/s Analog-To-Digital Converter," IEEE J. Solid-State Circuits, vol. 27, No. 3, pp. 351-358, March 1992.

[10] Thomas B. Cho, Paul R. Gray, "A 10-bit 20-MS/s, 35mW Pipeline A/D Converter," IEEE J. Solid State Circuits, vol. SC-30, No. 3, March 1995, p 166-172.

[11] S. Karthikeyan, S. Mortezapour, A. Tamineedi and E. K. F. Lee, "Low-Voltage Analog Circuit Design Based on Biased Inverting Opamp Configuration," IEEE Trans. Circuits Syst.-II, vol. 47, No. 3, pp. 176-184, Mar. 2000.