

A Stochastic Model for Interconnection Complexity based on Rent's Rule

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Abstract

In the past, Rent's rule has been successfully applied for a priori estimation of wire length distributions. Deviations to Rent's rule appear due to the existence of heterogeneity. This can be classified in hierarchical and spatial heterogeneity. Stochastic models for the interconnection complexity, based on Rent's rule, are introduced. A coarse model shows that the variance follows a power law relationship. A more refined model incorporates the effect of local spatial heterogeneity. Experiments show that this is sufficient to model the variance of the terminal count distribution. Finally, the model is further extended to incorporate global spatial heterogeneity.

1 Introduction

The interconnection complexity of a circuit is well captured by Rent's rule [1] and the corresponding Rent exponent. This rule has been applied numerous times, especially in the field of a priori wire length estimation [2, 3, 4]. Because of the absence of placement and routing information, it is impossible to accurately estimate the length of individual nets, but the wire length distribution can be predicted fairly accurately. Larger Rent exponents result in more flat wire length distributions, with relatively more long wires. This results in a larger average wire length and hence a larger total wiring area. Since the wiring area dominates the total area of contemporary chips, it seems valuable to include the Rent exponent in the cost objective during synthesis. Measurement of the Rent exponent seems fairly expensive, as it requires partitioning the circuit into smaller modules. But when using a divide-by-conquer approach for synthesis, the partitioning and thus the Rent exponent can be obtained "for free".

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Furthermore, a priori wire length estimation could be extremely valuable for the interaction between logic synthesis and physical design. During synthesis, tight wire length constraints can be set on the individual nets, which allows accurate delay estimation. Because of the accurate estimation of the wire length distribution, the wire length constraints can be met during the physical design stage. This approach could guarantee timing closure without requiring many design iterations.

Nevertheless many researchers remain suspicious about the use of Rent's rule: it is an empirical law that holds on average, but there are many cases where significant deviations exist. These deviations result mainly from heterogeneity in the circuit. Circuit heterogeneity comes in two forms: hierarchical heterogeneity and spatial heterogeneity. The former is well known and has been studied thoroughly [1, 3, 5, 6, 7]. The latter has had little attention so far – yet it is known to have a huge impact on the accuracy of wire length estimations based on Rent's rule [5]. Spatial heterogeneity results in spread on the Rent characteristic. As shown in [8], the amount of variance is a fundamental property of circuits, and has a direct influence on the difficulty of finding good partitionings of the circuit.

In this paper we will study the deviations from Rent's rule. After an overview of the basic definitions and Rent's rule in the next section, we will briefly discuss hierarchical heterogeneity. In section 4 we will focus on the spatial heterogeneity. First, a coarse model that takes the logic block degree distribution into account will be derived. This model will be refined to incorporate the effect of local spatial heterogeneity. Finally the model will be further extended to model global spatial heterogeneity as well.

2 Preliminaries

In this section we will give an overview of the basic definitions and we continue with a discussion on Rent's rule.

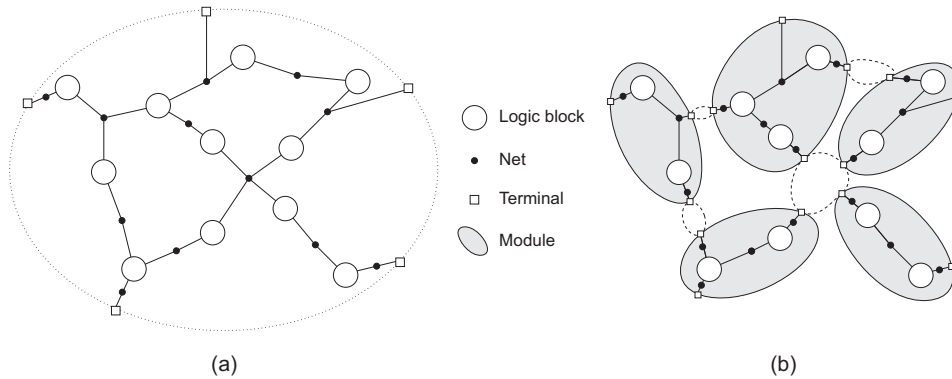


Figure 1: Model of a circuit (a) and the partitioning of the circuit into modules (b).

2.1 Definitions

A circuit can be represented by a set of interconnected *blocks*, as in figure 1(a) (the blocks can be the representation of transistors, gates or even entire circuits). An interconnection between two or more blocks is called a *net*. A net that is connected to more than two blocks is called a *multi-terminal net*. Some of the nets are also connected to the outside world. These nets are called *external nets*, as opposed to the *internal nets* which only connect blocks within the circuit. In order to model these external nets properly, we introduce a new kind of block which we call a *terminal*. The other blocks are called *logic blocks*. Every external net is connected to exactly one terminal. The *circuit size* is defined as the number of logic blocks contained by the circuit. The *terminal count* T corresponds to the number of terminals of the circuit. The *logic block degree* t is the number of nets incident to the logic block. The *logic block degree distribution* \mathcal{D}_t is the collection of values, indicating for each t , how many logic blocks have a logic block degree equaling t .

Partitioning a circuit means dividing this circuit into disjoint sub-circuits (called *modules*), each containing a subset of the blocks (figure 1(b)). Generally the criterion for partitioning is to minimize the number of nets cut, i.e. the number of nets crossing the borders of modules in the partition. Recently, it has been observed that minimizing the number of terminals is a better criterion than minimizing the number of nets cut and that both criteria are not equal for multi-terminal external nets [9]. Nets that are cut by module boundaries are shared between two or more modules and are said to be external to the modules. Therefore, the net is split into a number of sub-nets (if the net was already external to the circuit then the terminal assigned to it can be reused for one of the sub-nets). Each module itself can be seen as a circuit and can be partitioned further. A partitioning process where the modules themselves are recursively

partitioned is called a *hierarchical partitioning method*.

For a partition \mathcal{P} , the *terminal count distribution* $\mathcal{D}_T(\mathcal{P})$ is a collection of values, indicating for each terminal count T , how many modules have exactly T terminals. One usually considers partitions of more or less equally sized modules. These partitions are identified by the average module size \bar{B} , and the corresponding terminal count distribution is written as $\mathcal{D}_T(\bar{B})$. At the lowest level of a hierarchical partitioning of a circuit, where every module contains a single logic block, the terminal count distribution equals the logic block degree distribution, hence $\mathcal{D}_T(1) = \mathcal{D}_t$.

2.2 Rent's rule

Circuits can be classified according to their interconnection structure. These differences in complexity of the interconnection topology have been experimentally observed by Rent, and his observations have led to the well-known Rent's rule [1]. This law states that, when partitioning a circuit in a number of more or less equally sized modules, there exists a power law relationship between the average terminal count \bar{T} and the average number of logic blocks \bar{B} :

$$\bar{T} = k\bar{B}^p \quad (1)$$

Here, k corresponds to the average logic block degree \bar{t} , and p is the Rent exponent. The validity of this rule is a result of the *self-similarity* [11] that exists in real circuits. A high Rent exponent implies many global interconnections, and hence a high interconnection complexity. Generally, p ranges from 0.47 for regular circuits, such as Random Access Memories, up to 0.75 for complex circuits, such as fast full custom VLSI circuits [12]. The visualization of the terminal count distribution as function of the module size is called the *Rent characteristic*, as shown in figure 2).

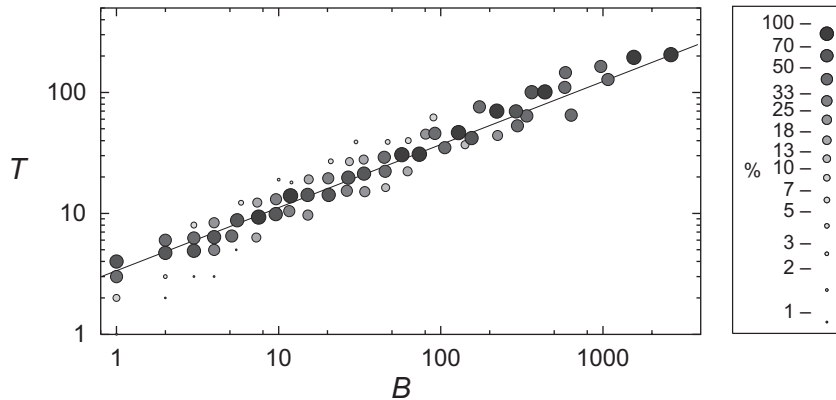


Figure 2: Rent characteristic of LGsynth93 [10] circuit apex5. The size of the circles corresponds to the percentage of modules that has T terminals and B blocks in a pool of modules around an average number of blocks.

Since partitioning algorithms are heuristic, the solution is not guaranteed to be optimal. As a result, the terminal count distribution and the resulting Rent exponent is not only determined by the circuit itself, but also depends on the partitioning algorithm [13]. The results obtained from these suboptimal partitions are still relevant, since similar partitioning schemes are used in contemporary placement tools. For the experimental results reported in this paper, we have used a recursive partitioning scheme, where at each hierarchical level the modules are bipartitioned using hMetis [14].

3 Hierarchical heterogeneity

While recursively partitioning a circuit, the observed Rent exponent may vary across the different levels of hierarchy. The deviation at the highest levels of hierarchy results in Rent region II [1], as opposed to region I, which is the region where (1) is valid. The deviation at the lowest levels results in Rent region III [6]. This piecewise linear approximation¹ of Rent’s rule models the hierarchical heterogeneity quite well, as shown in figure 3.

Region II At the highest levels of the hierarchy the number of terminals quite often appear to be lower than expected by (1). This behavior can be intrinsic to the functionality of the circuit, but is mostly due to technological and psychological constraints [7].

The most important technological constraint is the pin-limitation of contemporary packages. As a result, various coding techniques, such as time multiplexing and compression, are used in order to maximize the entropy that is transported across the circuit pins. A similar technological constraint exists for circuit submodules,

¹In the log-log domain.

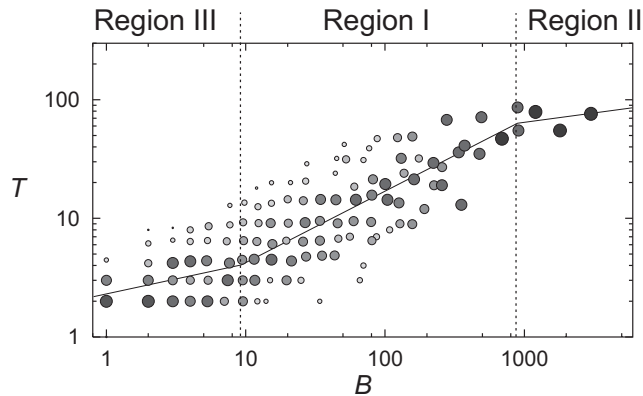


Figure 3: Rent characteristic for circuit s9234.1.

since these are interconnected through busses, and the number of bus lines should be minimized to minimize the total number of global wires. Quite often, designers are too much aware of these constraints. They are indoctrinated to use as little terminals as possible, which results in a psychological constraint.

Region III During the logic synthesis phase the circuit is mapped to a certain technology. The logic block degree distribution seems more or less independent from the circuit and is mainly determined by the logic blocks that are available in the technology. As a result, the average logic block degree, and thus the average terminal count for modules of size $B = 1$ (lowest level of the hierarchy) is mostly determined by the technology and mainly independent from the circuit and its complexity. When a mismatch exists between the average logic block degree and the k parameter in (1), which corresponds to Rent region I, a region III is observed.

The factor k is meaningless for the actual circuit com-

plexity. Consider the case where the logic blocks are simple logic gates, without macro cells such as IP cores. A typical average logic block degree would be $\bar{t} = 3.5$. Now look at the internals of the logic gates, which actually consist of transistors. Changing the viewpoint does not alter the circuit complexity, even though the average logic block degree is different. The Rent characteristic appears to be shifted to higher module sizes, but the Rent characteristic and the corresponding Rent exponent does not change significantly in Region I and II. Because of the smaller granularity, we expect the partitioning tool to find finer cuts, but apparently this only has influence on the lower levels of the hierarchy.

A similar effect appears when the circuit is mapped to different technologies: the Rent characteristics and corresponding Rent exponents (at least in Regions I and II) seem independent of the technology the circuit is mapped to during logic synthesis [15].

4 Spatial heterogeneity

For a priori wire length estimation, a simplified circuit model based on Rent's rule is frequently used. In this model one assumes that the terminal count for each module complies exactly to Rent's rule, i.e. the terminal count distributions are assumed to be concentrated at a single value given by Rent's rule.² In reality these distributions exhibit a certain spread, which is partly the result of the logic block degree distribution, but mainly determined by deviations from Rent's rule (spatial heterogeneity). Visually, when inspecting the Rent characteristics, the amount of spread seems to diminish for increasing block size, due to the compressing effect of the logarithmic scale. In reality the amount of spread, which can be characterized by the variance of the terminal count distribution, increases for increasing module size.

In this section we will model the influence of the logic block degree distribution. Then we will refine this model by adding spatial heterogeneity. We will focus mainly on the variance of the terminal count distribution, but we will briefly inspect the shape of the distributions as well.

4.1 Influence of the logic block degree distribution

For $B = 1$, i.e. the lowest level of hierarchy in a recursive partitioning scheme, the spread of the terminal count distribution is determined by the logic block degree distribution. Because of this distribution, we expect

²Rounded to the nearest integer.

a certain amount of spread at the other levels of the hierarchy ($B > 1$). This can be demonstrated with the following stochastic model.

Consider the opposite of recursive partitioning the circuit: the bottom-up clustering of the logic blocks into modules, and further combining those modules to a complete circuit. First consider the combination of two modules of identical size B and terminal count T into a new module with $B_c = 2B$ blocks and T_c terminals. Because of the self-similarity, the number of terminals that is reduced is determined by Rent's rule:

$$T_c = kB_c^p = k(2B)^p = 2^p T \quad (2)$$

The total terminal count before combination was $2T$, therefore in a single combination step the number of terminals is reduced by a factor α :

$$\alpha = \frac{T_c}{2T} = 2^{p-1} \quad (3)$$

Of course, because of the logic block degree distribution, the modules that are combined will not be identical. However, since the circuits are partitioned with a constraint on the maximum imbalance, the number of blocks will be similar. Experiments show that the allowed maximum imbalance does not fundamentally change the terminal count distribution.³

For modules with different terminal count, the fraction α is assumed to be independent of the true number of terminals, such that the number of terminals of a module at hierarchical level k , where $B = 2^k$, is given by:

$$\mathbf{T}(2^k) = \alpha^k (\mathbf{t}_1 + \mathbf{t}_2 + \dots + \mathbf{t}_{2^k}) \quad (4)$$

In this expression \mathbf{t}_i are random variables with distribution defined by the logic block degree distribution. Since every bipartitioning in the recursive partitioning scheme is performed locally, i.e. without considering the cost functions of the bipartitionings at the same and lower levels of the hierarchy, the \mathbf{t}_i variables in the reverse clustering scheme can be assumed to be mutually independent. The expected value and the variance of the terminal count distribution at hierarchical level k is then:

$$\mathbf{E}[\mathbf{T}(2^k)] = \alpha^k 2^k \mathbf{E}[\mathbf{t}] = 2^{kp} \mathbf{E}[\mathbf{t}] \quad (5)$$

$$\text{Var}[\mathbf{T}(2^k)] = \alpha^{2k} 2^k \text{Var}[\mathbf{t}] = 2^{(2p-1)k} \text{Var}[\mathbf{t}] \quad (6)$$

Since the logic block degree distribution is fixed, the expected value and variance can easily be measured as the mean \bar{t} and sample variance σ_t^2 of this distribution. Substituting for the module size B we get:

$$\mathbf{E}[\mathbf{T}(B)] = B^p \bar{t} \quad (7)$$

$$\text{Var}[\mathbf{T}(B)] = B^{(2p-1)} \sigma_t^2 \quad (8)$$

The first expression reduces to Rent's rule with $k = \bar{t}$. When the Rent exponent $p > 0.5$, the variance increases.

³At least not when using an advanced partitioning algorithm such as hMetis.

For $p = 0.5$, the variance remains constant, and for $p < 0.5$ it decreases. Figure 4 shows actual and predicted variance for ISPD98 circuit `ibm02`, which has a Rent exponent of 0.705. The existence of a power law relationship is confirmed, but the measured exponent does not comply with (7). Of course the measurement of the Rent exponent is not exact, but in this case a Rent exponent of 1.114 would be required to obtain a fairly good match. This is nonsense, since a Rent exponent can never exceed 1. This indicates that the influence of the logic block degree distribution is only minor, and that the model needs further refinement.

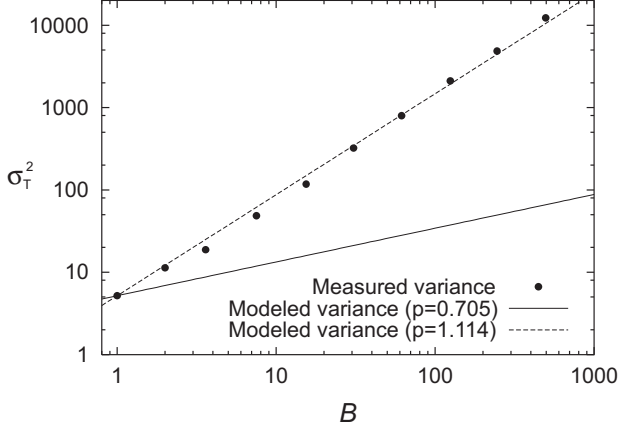


Figure 4: Measured and predicted variance for circuit `ibm02` (modeled without local heterogeneity).

4.2 Local spatial heterogeneity

In the previous model, we considered the factor α to be constant. In reality, this factor will also be a random variable, with mean $\bar{\alpha} = 2^{p-1}$ and variance σ_α^2 determined by the amount of local variety in the self-similarity. As a result, the variance of the terminal count distribution will increase much faster.

$$\mathbf{T}(2^k) = \alpha (\mathbf{T}_1(2^{k-1}) + \mathbf{T}_2(2^{k-1})) \quad (9)$$

Assume α , $\mathbf{T}_1(2^{k-1})$ and $\mathbf{T}_2(2^{k-1})$ to be stochastically independent. The expected value and the variance of the terminal count distribution becomes:

$$\mathbf{E}[\mathbf{T}(2^k)] = 2\mathbf{E}[\alpha]\mathbf{E}[\mathbf{T}(2^{k-1})] \quad (10)$$

$$\begin{aligned} \text{Var}[\mathbf{T}(2^k)] &= 2\text{Var}[\alpha]\text{Var}[\mathbf{T}(2^{k-1})] \\ &\quad + 4\text{Var}[\alpha]\mathbf{E}[\mathbf{T}(2^{k-1})]^2 \\ &\quad + 2\text{Var}[\mathbf{T}(2^{k-1})]\mathbf{E}[\alpha]^2 \end{aligned} \quad (11)$$

Solving these recursive relationships yields:

$$\mathbf{E}[\mathbf{T}(2^k)] = 2^k \mathbf{E}[\alpha]^k \mathbf{E}[\mathbf{T}(1)] = 2^k \mathbf{E}[\mathbf{t}] \quad (12)$$

$$\text{Var}[\mathbf{T}(2^k)] = \text{Var}[\mathbf{T}(1)] (2\mathbf{E}[\alpha]^2 + 2\text{Var}[\alpha])^k$$

$$\begin{aligned} &+ \frac{2\text{Var}[\alpha]\mathbf{E}[\mathbf{T}(1)]^2}{\mathbf{E}[\alpha]^2 - \text{Var}[\alpha]} \left((4\mathbf{E}[\alpha]^2)^k \right. \\ &\quad \left. - (2\mathbf{E}[\alpha]^2 + 2\text{Var}[\alpha])^k \right) \\ &= \left(\text{Var}[\mathbf{t}] - \frac{2\sigma_\alpha^2}{\bar{\alpha}^2 - \sigma_\alpha^2} \mathbf{E}[\mathbf{t}]^2 \right) (2\bar{\alpha}^2 + 2\sigma_\alpha^2)^k \\ &\quad + 4 \frac{2\sigma_\alpha^2}{\bar{\alpha}^2 - \sigma_\alpha^2} \mathbf{E}[\mathbf{t}]^2 \bar{\alpha}^{2k} \end{aligned} \quad (13)$$

After substituting for the module size $B = 2^k$ this results in:

$$\mathbf{E}[\mathbf{T}(B)] = B^p \bar{t} \quad (14)$$

$$\begin{aligned} \text{Var}[\mathbf{T}(B)] &= \left(\sigma_t^2 - \frac{2\sigma_\alpha^2}{\bar{\alpha}^2 - \sigma_\alpha^2} \bar{t}^2 \right) B^{1+\log_2(\bar{\alpha}^2 + \sigma_\alpha^2)} \\ &\quad + \frac{2\sigma_\alpha^2}{\bar{\alpha}^2 - \sigma_\alpha^2} \bar{t}^2 B^{2p} \end{aligned} \quad (15)$$

Expression (14) is again Rent's rule. The variance consists of two terms. Since $\alpha \in [0, 1]$ and for $p > 0.4$, $\bar{\alpha} > 0.66$, the variance σ_α^2 will always be significantly smaller than $\bar{\alpha}^2$. Therefore the exponent of the first term will be approximately $2p - 1$, such that the second term will dominate for sufficiently large module size.

Figure 5 shows the variance for circuit `ibm01`. The rent exponent of 0.588 results in a fairly good fit for the variance, but a much better fit can be obtained with rent exponent of 0.805. This is probably due to global heterogeneity, which will be discussed further.

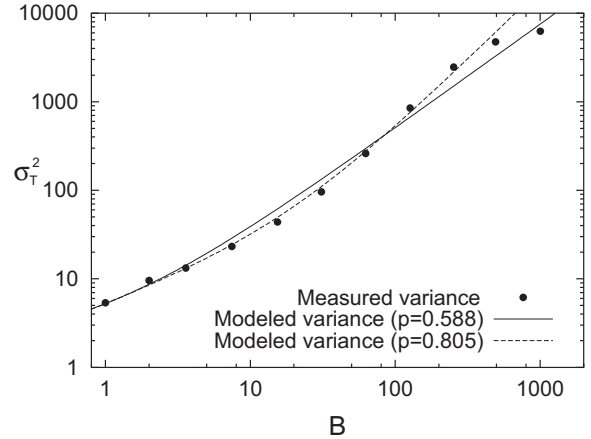


Figure 5: Measured and predicted variance for circuit `ibm01` (modeled with local heterogeneity). The parameter σ_α^2 was obtained by optimizing for best fit.

In table 1 the results for all ISPD98 circuits are shown. For each circuit expression (15) is fitted twice: in the first case the Rent exponent p is fixed to the measured value, and only the variance σ_α^2 is optimized; in the second case both p and σ_α^2 are optimized. In both cases the average

Circuit	Fixed p			Optimized p		
	p	σ_α^2	Error	p	σ_α^2	Error
ibm01	0.588	0.036	0.0133	0.805	0.006	0.0018
ibm02	0.705	0.038	0.0031	0.662	0.052	0.0011
ibm03	0.659	0.067	0.0097	0.581	0.114	0.0042
ibm04	0.676	0.086	0.0625	0.364	0.382	0.0057
ibm05	0.715	0.045	0.0190	0.621	0.091	0.0040
ibm06	0.632	0.040	0.0047	0.650	0.034	0.0040
ibm07	0.645	0.070	0.0044	0.669	0.058	0.0036
ibm08	0.632	0.111	0.0706	0.399	0.390	0.0042
ibm09	0.604	0.062	0.0080	0.569	0.083	0.0061
ibm10	0.631	0.063	0.0219	0.540	0.133	0.0025
ibm11	0.629	0.056	0.0108	0.582	0.084	0.0075
ibm12	0.654	0.102	0.0356	0.531	0.243	0.0066
ibm13	0.630	0.066	0.0109	0.566	0.111	0.0037
ibm14	0.628	0.076	0.0360	0.504	0.195	0.0022
ibm15	0.630	0.085	0.0088	0.588	0.122	0.0036
ibm16	0.620	0.075	0.0070	0.577	0.107	0.0023
ibm17	0.661	0.060	0.0021	0.659	0.061	0.0021
ibm18	0.612	0.104	0.0240	0.707	0.050	0.0031

Table 1: Variance fit for ISPD98 benchmark circuits.

logarithmic error is minimized. Except for a few circuits, such as `ibm04` and `ibm08`, the model allows a good fit, especially when the Rent exponent is adjusted as well.

4.3 Global spatial heterogeneity

So far we only analyzed the variance of the terminal count distributions. For some applications the actual shape of the distributions could be important. In the previously derived model, the terminal count at each hierarchical level is a sum of random variables. Because of the shared α factors, these random variables are not mutually independent. Hence, the central limit theorem does not apply, and the shape of the terminal count distributions will depend on the distribution of α .

We inspected the normalized terminal count distribution for a variety of logic block degree distributions and α distributions. According to our model, the terminal count distribution converges quickly to a distribution that seems bell-shaped, but is skewed towards smaller terminal counts. The terminal count distributions of most large ISPD98 circuits seem to have a similar shape. This shape is shown in figure 6(b). Note that it is actually quite hard to measure the terminal count distribution of real circuits, since the number of sample points decreases exponentially due to the recursive partitioning scheme.

Some of the smaller ISPD98 circuits converge to a platykurtic distribution, i.e. a flat topped distribution, or even a multimodal distribution, as shown in figure 6(a) for circuit `ibm01`. This indicates that the circuits are actually a mixture of different sub-circuits, each with different Rent exponent. This global spatial heterogeneity exists in many circuits. It is either introduced by the designer (example: a circuit that consists of a controller,

datapath and memory), or by the synthesis tool (example: a fast multiplier that consists of a Wallace tree of carry-save adders and a fast carry-lookahead adder).

When hierarchically partitioning a global heterogeneous circuit, the heterogeneity will become apparent at the highest levels of the hierarchy: the circuit falls apart into smaller sub-circuits that are globally homogeneous. This can easily be incorporated into the stochastic model, since the global heterogeneity determines a partitioning of the logic blocks into distinct classes. When clustering the different logic blocks and resulting modules, only those logic blocks and modules that consist of the same class can be combined.

The resulting terminal count distributions are a mixture of distributions that correspond to global homogeneous circuits. Consider a global heterogeneous circuit that consists of n sub-circuits of size B_1, B_2, \dots, B_n , with corresponding terminal count distributions $\mathcal{D}_{T_1}, \mathcal{D}_{T_2}, \dots, \mathcal{D}_{T_n}$. The terminal count is then given by:

$$\mathbf{T}(B) = \mathbf{T}_{\mathbf{j}}(B) \quad (16)$$

where \mathbf{j} is a discrete random variable with distribution defined by the size of the sub-circuits:

$$\mathcal{D}_{\mathbf{j}} = \frac{B_{\mathbf{j}}}{B_1 + B_2 + \dots + B_n} \quad (17)$$

The calculation of the expected value and variance is straightforward:

$$\mathbf{E}[\mathbf{T}(B)] = \sum_{i=1}^n \mathcal{D}_i \mathbf{E}[\mathbf{T}_i(B)] \quad (18)$$

$$\begin{aligned} \text{Var}[\mathbf{T}(B)] &= \sum_{i=1}^n \mathcal{D}_i \mathbf{E}[\mathbf{T}_i(B)^2] - \mathbf{E}[\mathbf{T}(B)]^2 \\ &= \sum_{i=1}^n \mathcal{D}_i (\text{Var}[\mathbf{T}_i(B)] + \mathbf{E}[\mathbf{T}_i(B)]^2) \\ &\quad - \mathbf{E}[\mathbf{T}(B)]^2 \end{aligned} \quad (19)$$

From the last expression it is clear that the variance consists of multiple terms. When substituting (14) and (15) for $\mathbf{E}[\mathbf{T}_i(B)]$ and $\text{Var}[\mathbf{T}_i(B)]$, we get a sum of exponential terms. Thus global heterogeneity adds degrees of freedom to the stochastic model, but does not fundamentally change the nature of the expression for the variance. The extra degrees of freedom will obviously result in a better fit, but the gain seems only marginal, since a fairly good fit was already obtained with the previous model.

5 Conclusion

Deviations to Rent's rule appear due to the existence of heterogeneity. Hierarchical heterogeneity can be mod-

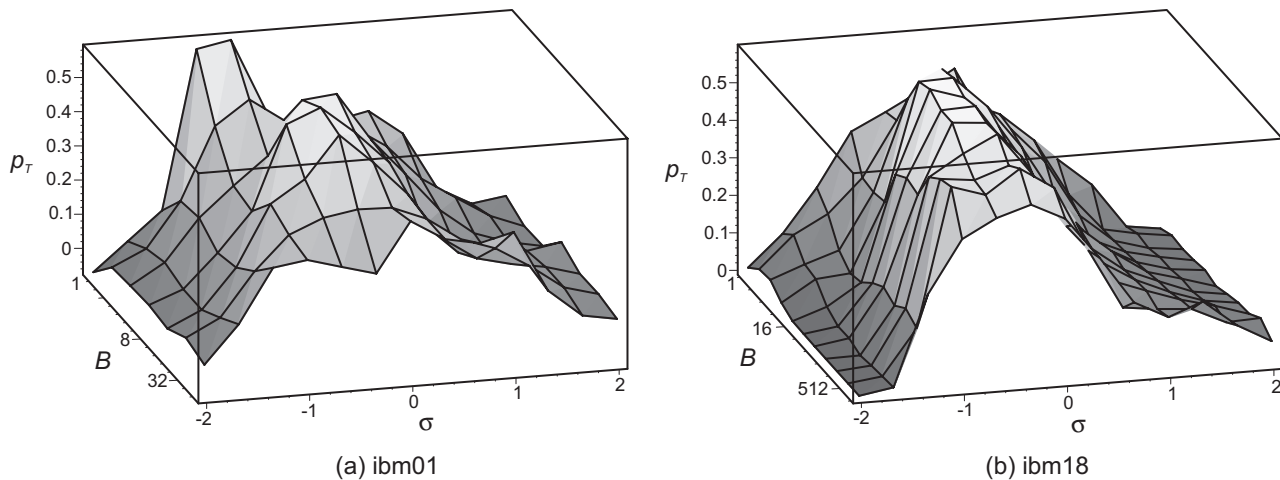


Figure 6: Normalized terminal count distribution for circuits ibm01 and ibm18.

eled by splitting up Rent's rule in different regions according to the module size, which results in a piecewise linear approximation of Rent's rule. The terminal count distribution exhibits a certain amount of spread, which is partly the result of the logic block degree distribution, but mainly due to spatial heterogeneity.

A coarse model for the terminal count distribution has been derived to take the logic block degree distribution into account. This model was further refined to account for the local spatial heterogeneity. The result is a simple yet accurate model that is sufficient to describe the variance of the terminal count distribution quite accurately.

Further extensions are possible to incorporate the effects of global spatial heterogeneity. This results in a more complex model that is capable of describing both the variance and the shape of the terminal count distribution.

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