On an Efficient Method for Estimating the Interconnection Complexity of Designs and on the Existence of Region III in Rent's Rule

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Abstract

The interconnection complexity of digital designs can be captured by the well-known Rent exponent, described by Landman and Russo [2]. In this paper, we present an efficient method for obtaining the Rent exponent of a design through a hierarchical partitioning algorithm. Experimental results not only confirm the Landman and Russo observations of a region I and region II, but also show a hitherto unknown region III.

1. Introduction

The production of VLSI computer chips requires the layout (placement and routing) of the chip design on a carrier. For obtaining a good layout, a priori estimation of important layout properties (such as wire length) is essential [3].

For obtaining valuable a priori estimations, one should have a notion of the interconnection complexity of the design. This interconnection complexity can be described by a fundamental equation which is known as Rent's rule [2]. It relates the number of logic blocks B in a module of a partitioned design to the number of the module's external connections (pins) P: $P = T_b\, B^r$, where T_b is the average number of terminals per logic block, and r is called the *Rent exponent*. Rent's rule can be observed by partitioning a circuit and plotting the number of pins per module versus the number of blocks per module in a log-log plot (as in figure 1).[1]

In this paper, we use the `ratio cut` partitioning method [5] to obtain the Rent exponent efficiently. Our results confirm the observations made by Landman and Russo and reveal a hitherto unknown deviation from Rent's rule.

*The author is Postdoctoral Fellow of the Fund for Scientific Research of Flanders (Belgium) (F.W.O.).

[1] The size of the circles corresponds to the percentage of modules that has P pins and B blocks in a pool of modules around an average B.

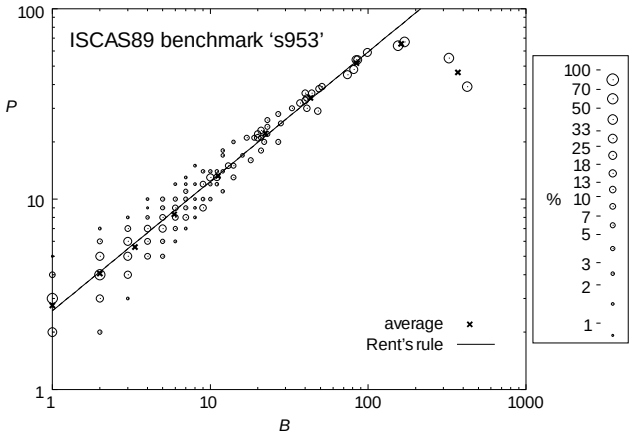

Figure 1. Number of pins versus number of blocks for every module in ratio cut.

2. Using ratio cut partitioning

In [2], Landman and Russo described an algorithm for finding the Rent exponent of a design. This algorithm is very time-consuming since the whole design has to be partitioned multiple times, in subsequently smaller modules. However, experiments show that the Rent exponent can also be found by a 'good' hierarchical partitioning method [1]. Moreover, a partitioning of the circuit is generally performed before the layout step in the design process so the calculation of the Rent exponent can be obtained for free. The heurisitic partitioning methods are also significantly faster than Landman and Russo's algorithm. `Ratio cut` [5] is found to be one of the best hierarchical partitioning algorithms [1] and is often used. Therefore, a good partitioning tree as well as a good estimate of the interconnection complexity can be obtained at the same time by using the `ratio cut` partitioning method.

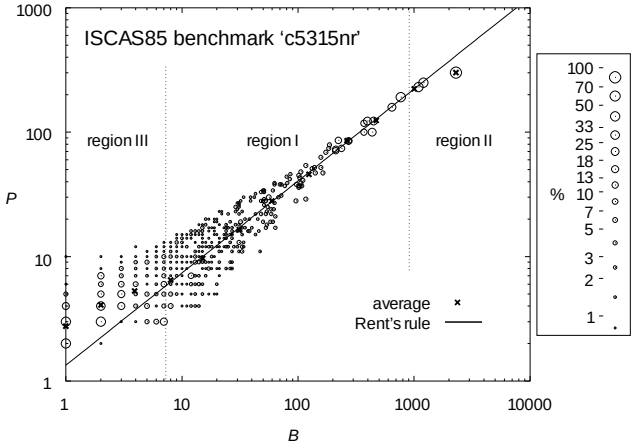

Figure 2. Number of pins versus number of blocks for every module in ratio cut.

3. Region III in Rent's rule

We improved `ratio cut` [4] and implemented an automatic fit to Rent's rule by a least squares fit on average P-values, for B-values an equal distance apart. The averages are taken in the logarithmic domain which is far more natural than the linear averaging used in [2]. Two results are shown in figures 1 and 2. As observed by Landman and Russo, the data points seem to follow Rent's rule quite good over a wide range. However, for large values of P and B, the number of pins is generally much lower than is predicted by Rent's rule. For this region, Landman and Russo introduced the name *region II* (against the 'normal' *region I*). The lower number of pins in region II results from the fact that designers need to alleviate pin constraints by lowering the number of pins at the higher partitioning levels.

Our results with the (extended) `ratio cut` partitioning algorithm confirm the existence of both regions I and II. However, for some designs, we also find a deviation at the other end of the scale. For small module sizes, the number of pins seems to be higher than the value predicted by Rent's rule (figure 2). For this deviation, we introduce *region III*. We believe that the deviation in region III is the result of a mismatch between the number of terminals per logic block (which represents the *local interconnection complexity* around that logic block) and the *global interconnection complexity* (as observed through Rent's rule). We have shown that this mismatch exists for several benchmark circuits [3]. The number of interconnections that can be laid is limited by the number of terminals that can drive a net, i.e., by the number of block outputs. In most designs, the logic blocks have one output but several input terminals. If the number of input terminals is too high, a mismatch exists between the *available interconnection complexity* and the *desired interconnection complexity*. Only for larger modules, the number of module inputs (also capable of driving nets) is sufficiently high to increase the interconnection complexity.

4. How to describe deviations from Rent's rule?

Deviations from Rent's rule at various hierarchical levels are combined in the notion of *hierarchical locality*. In [3], we presented a possible extension of Rent's rule to include local variations in interconnection complexity. Let the Rent exponent depend on the hierarchical level (or the average number of blocks per module) $P = T_b\, B^{r(B)}$. It then becomes an *incremental Rent exponent*, defined by the slope of the curve that connects, in a log-log plot, all pairs (B,P) for average modules: $r\,(B) = \partial \log(P) / \partial \log(B)$. This incremental Rent exponent can be used for describing Rent's rule in both region II and our newly observed region III.

5. Conclusion

A priori estimations of important layout properties of digital designs require a good understanding of their interconnection complexity and hence a good Rent exponent estimate. In this paper, we showed that the (standard) `ratio cut` partitioning algorithm is an efficient method for finding the Rent exponent. Experiments also revealed a hitherto unknown deviation from Rent's rule for small module sizes. The ability to recognize differences in interconnection complexity is important since the results of a priori estimations highly depend on the interconnection complexity. The notion that this complexity varies over the hierarchical levels warns us to use different estimates for the different levels.

References

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