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# A Digital Error-Averaging Technique for Pipelined A/D Conversion

P. Rombouts and L. Weyten

***Abstract*— Capacitor mismatch is the main source of nonlinearity for pipelined analog-to-digital (A/D) converters. Here a digital error-averaging technique is presented to greatly reduce this effect. Compared to the conventional circuit, the new approach requires only one extra digital addition. This allows a very simple and compact implementation. On the other hand, the conversion speed is halved because one conversion now requires two clock cycles instead of one. Therefore this technique is most suitable when moderately high speed combined with high resolution is required.**

***Index Terms*— Analog signal processing, analog-to-digital conversion, circuit techniques.**

## I. Introduction

At present the requirements for A/D converter circuits are rapidly increasing. Many applications demand both a multi-megahertz conversion rate and a linearity beyond 10 bit. An approach to achieve this, is to combine multistep and pipelining techniques. Here the effect of comparator inaccuracy can easily be eliminated by incorporating some redundancy in the decision circuit. A successful algorithm is the redundant signed digit (RSD) technique [1], [2]. However, linearity still remains limited due to component mismatch. Several methods to overcome this problem have been presented. One strategy is to provide the circuit with a self-calibration capability (e.g., [3]–[7]). This approach has the disadvantage that usually a significant amount of additional hardware is required. Also the need for periodic recalibration may be a disadvantage to the user. Other techniques use analog error averaging [8], [9]. These methods require a considerable increase in analog circuitry. Here a new digital error averaging technique is proposed. On the analog side, merely a few additional switches are introduced. Only one digital addition is needed for the error averaging. Therefore this method is suitable when high resolution combined with small chip area and power consumption are desired. However, this is achieved by halving the conversion speed, as will be seen in Section III.

In [10] another correction technique which allows a compact implementation, is introduced. Just like our new approach, it does not require a calibration cycle. While that method, however, does not halve the conversion speed, it corrects only differential nonlinearity, whereas the digital error averaging technique corrects both differential and integral nonlinearity.

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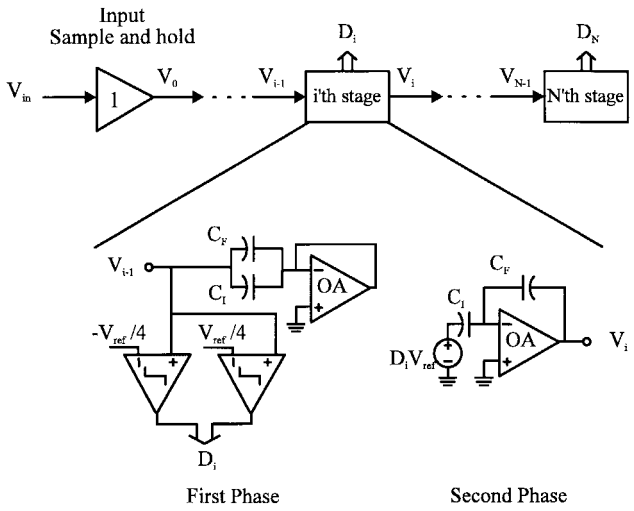



Fig. 1. Diagram of the conventional switched-capacitor A/D converter.

## II. Conventional Pipelined A/D Converter

In Fig. 1, a diagram of the conventional pipelined analog-to-digital (A/D) converter is shown [1]. For simplicity a single-ended circuit is shown although an actual implementation should be fully differential. The converter consists of an input sample and hold amplifier, followed by $N$ identical stages, with $N$ the total number of bits. Each stage performs the RSD A/D conversion as follows. In the sampling phase the output voltage of the previous stage $V_{i-1}$ is sampled on the capacitors $C_I$ and $C_F$. Meanwhile the two comparators generate the stage's output code $D_i = -1,\ 0$ or 1. In the second phase the capacitor $C_F$ is switched in the opamp's feedback loop while $C_I$ is switched to ground or $\pm V_{\rm ref}$ depending on the value of the code $D_i$ [2]. If $C_I$ and $C_F$ are perfectly matched, this can be described by

$$V_i = 2V_{i-1} - D_i V_{\rm ref}. \tag{1}$$

Through successive application of (1) we can rewrite the input voltage of the pipeline $V_0$ as

$$V_0 = \sum_{i=1}^{N} 2^{-i} D_i V_{\rm ref} + 2^{-N} V_N. \tag{2}$$

Now the conversion result $CR$ equals

$$CR = 2^N \sum_{i=1}^{N} 2^{-i} D_i. \tag{3}$$

## III. Digital Error-Averaging

In a practical implementation the $C_I$ and $C_F$ of the $i$th stage have a mismatch $\varepsilon_i$:

$$C_I = C_F(1 + \varepsilon_i) \tag{4}$$

and therefore in the real converter:

$$V_i' = (2 + \varepsilon_i)V_{i-1}' - (1 + \varepsilon_i)D_i' V_{\rm ref}. \tag{5}$$

Let us now assume that the linearity of the uncorrected pipelined A/D converter is limited to $n$ bits due to capacitor mismatch. We will consider an $N = m + n$ bit pipelined A/D converter.

Let $V'_m$ denote the output residue voltage of the $m$th stage. It is clear that $V'_m$ will depend on the value of the capacitor mismatches of the first $m$ stages. Now we can express this dependence as a Taylor series. Since the $\varepsilon_i$ are expected to be small, we need to the consider only first-order terms in the $\varepsilon_i$. Then we can write

$$V'_m = 2^m V_0 - 2^m \sum_{i=1}^{m} 2^{-i} D'_i V_{\rm ref} + \sum_{i=1}^{m} a_i \varepsilon_i. \tag{6}$$

The coefficients $a_i$ depend on the $D'_i$'s, and also on the input voltage $V_{\rm in}$. This residue voltage $V'_m$ is converted by the $n$ tail stages that generate the output codes $D'_{m+1} \cdots D'_N$. Now we can write similarly as in (2):

$$V'_m = \sum_{i=m+1}^{N} 2^{-i+m} D'_i V_{\rm ref} + 2^{-n} V'_N + V_{\rm ref} \varepsilon'. \tag{7}$$

Here the last term $V_{\rm ref}\varepsilon'$ represents the error resulting from capacitor mismatch in the $n$ tail stages of the pipeline.

In the following two phases the role of all the $C_I$ and $C_F$ capacitors in the first $m$ stages is interchanged. The first stage input voltage $V_0$ is kept constant by the input sample and hold circuit, and the codes $D'_1 \cdots D'_m$ of the previous case are stored and reused. This means that the comparators of the first $m$ stages are not used. Then the residue voltage $V''_m$ is generated at the output of the $m$th stage. Again by making a Taylor expansion and collecting first order terms in the $\varepsilon_i$ we obtain

$$V''_m = 2^m V_0 - 2^m \sum_{i=1}^{m} 2^{-i} D'_i V_{\rm ref} - \sum_{i=1}^{m} a_i \varepsilon_i. \tag{8}$$

Here the error contribution has exactly the opposite sign as in (6). This can be understood from (4). Indeed, interchanging the role of $C_I$ and $C_F$ corresponds to replacing $(1+\varepsilon_i)$ with $(1+\varepsilon_i)^{-1}$. Since only first order terms in $\varepsilon_i$ are considered, this is equivalent with replacing $\varepsilon_i$ with $-\varepsilon_i$.

This residue voltage is converted by the $n$ tail stages of the converter, that now generate the output codes $D''_{m+1} \cdots D''_N$:

$$V''_m = \sum_{i=m+1}^{N} 2^{-i+m} D''_i V_{\rm ref} + 2^{-n} V''_N + V_{\rm ref} \varepsilon''. \tag{9}$$

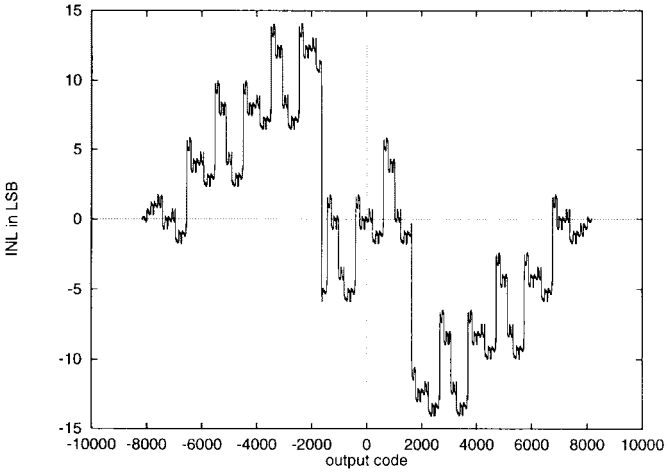
Again $V_{\rm ref}\varepsilon''$ represents the error resulting from capacitor mismatch in the $n$ tail stages of the pipeline. Combining (6)–(9), we obtain

$$V_0 = \sum_{i=1}^{m} 2^{-i} D'_i V_{\rm ref} + \frac{1}{2} \sum_{i=m+1}^{N} 2^{-i} (D'_i + D''_i) V_{\rm ref} + 2^{-N} \frac{(V'_N + V''_N)}{2} + V_{\rm ref} 2^{-m} \frac{(\varepsilon' + \varepsilon'')}{2}. \tag{10}$$

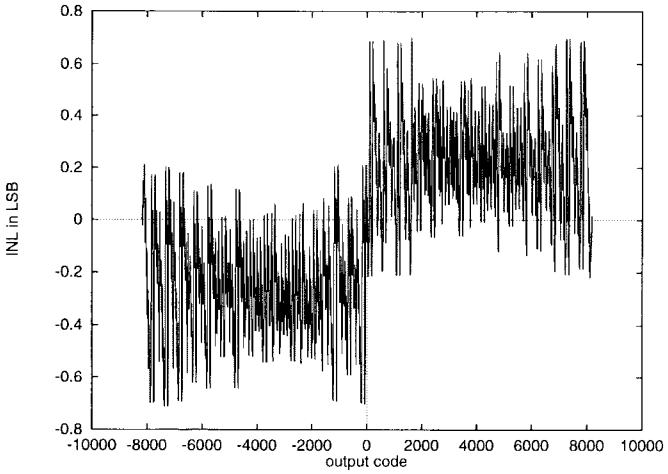
Now we have the digital averaged conversion result $CR$:

$$CR = 2^N \left[ \sum_{i=1}^{m} 2^{-i} D'_i + \frac{1}{2} \sum_{i=m+1}^{N} 2^{-i} (D'_i + D''_i) \right]. \tag{11}$$

Comparing this with (10) we see that the effect of capacitor mismatch in the first $m$ stages is eliminated. The effect of mismatch in the $n$ tail stages remains but is reduced by the total gain of the preceding stages.




(a)




(b)

Fig. 2. Integral nonlinearity versus output code for a 14-bit A/D converter. (a) Without digital error averaging. (b) With digital error averaging.

Summarizing, the corrected pipeline operates at the same clock frequency as the uncorrected pipeline but at half its sampling rate. Now, four clock phases are needed instead of two: two for the straight conversion and two for the opposite error generation and conversion. From (11) it is also clear that only one supplementary addition is required. The division by two can be implemented by simply truncating the last bit. However, this introduces a truncation error, however.

## IV. Accuracy Considerations

In the previous section, we have concluded that the error contribution of terms of first order in the capacitor mismatch has been eliminated. However, in (6)–(10) the contribution of second order terms was neglected. Since $n$-bit matching means that the $\varepsilon_i \approx 2^{-n}$, second order terms will have a magnitude of $\approx 2^{-2n}$. This means that at most about $2n$-bit performance can be obtained with this technique. Therefore, we can conclude that the number of corrected stages $m$ should not be larger than $n$. A more stringent condition on the number of stages that can be corrected, comes from the fact that $V''_m$ must not exceed the input range of the $(m+1)$th stage. The RSD algorithm provides a correction range of about $\pm(V_{\rm ref}/2)$ [1], [2], of which a part is already used to correct opamp and comparator offsets. Monte

Carlo simulations point out that this condition is met for offsets of upto $V_{\rm ref}/8$, when $m$ is taken two bits less than $n$.

In an actual circuit implementation not only capacitor mismatch will limit the performance of the converter. Also finite operational amplifier gain, charge injection from the switches and noise will reduce the achievable resolution. The finite-gain effect can only be eliminated by the use of high gain opamps, while noise and charge injection should be tackled through sound analog design.

## V. Simulations

In order to verify these theoretical results, a fully differential behavioral model of the A/D converter was implemented. Several simulations were performed for various values of capacitor matching and comparator offsets. All simulations were in full agreement with the previous discussion.

As an example typical INL results are plotted for a 14-bit converter without [Fig. 2(a)] and with [Fig. 2(b)] error-averaging. Capacitor mismatch was set arbitrarily to $\pm 0.4\%$ corresponding to $n = 8$ bit matching. The number of corrected stages $m$ was taken equal to 6. Comparator offsets were $\pm V_{\rm ref}/10$. The division by two of (11) is done by truncation. It can be seen that the INL is improved by a factor of more that 16.

## VI. Conclusion

In this paper a new digital error-averaging approach for pipelined A/D conversion is presented. Compared to the conventional circuit, the new method requires very little extra circuitry. Only the hardware to perform the addition of (10) is needed. That can be achieved with one digital adder and $n$ latches. This allows a very compact implementation. However the conversion speed is halved. Therefore, this technique is most suitable when moderately high speed combined with high resolution and small chip area are required.

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# A Simulator Core for Charge-Pump PLL's

Patrik Larsson

***Abstract*—Three techniques are introduced to enhance simulation speed of communication systems including a charge-pump phase-locked loop. First, a technique using exact explicit solutions of differential equations is extended to nonuniformly sampled circuits. This allows arbitrarily large time and voltage steps in an event-driven simulator without introducing numerical errors. Then, event prediction using mathematical limits enables large time steps and unlimited accuracy. Finally, an interpolator is combined with delay-partitioning to reduce the required oversampling rate. High accuracy is demonstrated with as low as four events per cycle of the system clock and an oversampling ratio of 3.**

***Index Terms*—Circuit simulation, discrete event simulation, interpolation, phase-locked loops, simulation, switching circuits, synchronization, time-varying circuits.**

## I. Introduction

Many communication systems contain digital signal processing blocks whose behavior can be accurately modeled using high-level functional simulations. However, timing recovery and clock generation are frequently implemented using mixed-signal phase-locked loops (PLL's), requiring continuous-time analog simulation. Timing recovery simulations also need to deal with widely varying time constants. To study the influence of jitter on an equalizer, full-system simulations must be run for several thousands or millions of symbols. At the same time, jitter simulations require a time-domain resolution greater than the expected cycle-to-cycle phase variation, equivalent to a fraction of a clock period.

The proposed simulation techniques will be applied to the system in Fig. 1. The Shaping Filter [digital finite impulse response (FIR)] and the digital/analog (D/A) converter are clocked by a transmit clock $\phi_T$ whereas the receiver clocked by $\phi_R$, is derived by a clock recovery circuit. The *Channel Model* is an FIR filter derived from measurements of a real channel. First, simulation of the PLL containing analog nodes is considered and then a technique to enhance the accuracy of the interaction between the two clock domains is presented.

## II. Simulation of Charge-Pump PLL's

### A. Terminology

The PLL model in [1] is extended to include multiple charge-injection as in Fig. 2. The charge pump is controlled by, for example, a nonlinear phase frequency detector (NPFD) [2], but any other switched phase detector is easily implemented. $x_2$ and $x_3$ represent

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