

On the Characterization of Multi-point Nets in Electronic Designs

Dirk Stroobandt*

ELIS Department
University of Ghent
B-9000 Gent, Belgium
dstr@elis.rug.ac.be

Fadi J. Kurdahi

ECE Department
University of California, Irvine
Irvine, CA-92697
kurdahi@ece.uci.edu

Abstract

Important layout properties of electronic designs include interconnection length values, clock speed, area requirements, and power dissipation. A reliable estimation of those properties is essential for improving placement and routing techniques for digital circuits.

Previous work on estimating design properties failed to take multi-point nets into account. All nets were assumed to be 2-point nets (especially for estimating the number of nets). In this paper, we aim at characterizing multi-point nets in electronic designs. We will develop a model for the behaviour of multi-point nets during the partitioning process. The resulting distribution of nets over their net degree will be validated through comparison with benchmark data.

1 Introduction

The production of VLSI and ULSI computer chips requires the layout (placement and routing) of the chip design on a carrier. With the advent of high level description languages such as VHDL, with the extensive use of component libraries, and with the standardization of production parameters, more and more steps in the design cycle are being automated. In the early days of chip design, manually designing a chip was still feasible. Nowadays, computer aided design (CAD) tools are indispensable to cope with the complexity and the limited time resources.

For the very high demands put on system performances these days, CAD tools often lack enough flexibility. The helping hand of expert system designers is still needed to make important design decisions. Especially for the placement and routing phases extremely high demands are set. For the placement and routing to be good enough, accu-

rate predictions of system performances are badly needed to limit the search in the vast solution space. CAD tools therefore use estimator tools [1, 4, 8, 9, 10, 11], usually based on partitioning methodologies [2].

The main design parameters that have to be estimated are the interconnection length within the placed design, area occupancy, clock frequency, power dissipation, and (especially for FPGA's) channel densities. The estimation can be performed before the design is actually placed and then used to obtain better layouts [9]. The estimates can also be used for gaining a more fundamental insight in the placement of designs on different carriers. A lot of research performed by Van Marck and Stroobandt is aimed at evaluating three-dimensional architectures where optical channels are used for the third dimension interconnections [8, 11, 13]. The possibilities of such architectures can be explored without the need to actually produce the systems.

A lot of effort has already been spent on the estimation of certain design parameters [1, 4, 8, 9, 10, 11]. However, none of the currently developed estimation techniques takes multi-point nets into account in general (although, for specific nets, a Steiner tree approximation is sometimes used). The goal of this paper is to characterize these multi-point nets. After a general overview of the model for the design and the partitioning process in section 2, we will search for a way to model the behaviour of multi-point nets during partitioning. The obtained distribution of nets over the net degree will be evaluated by comparing them to experimentally measured distributions.

2 Design and partitioning models

Theoretical estimates that are valid for large classes of designs require some basic theoretical models. First of all, the design itself has to be modelled in such a way that the model is applicable to a large set of realistic designs. Secondly, we have to model the partitioning process for a design. Each of these models will be explained in this section.

*The author is Research Assistant of the Fund for Scientific Research - Flanders (Belgium) (F.W.O.).

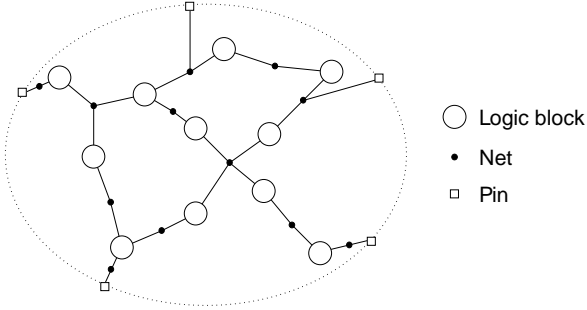


Figure 1. Model of a design.

A design can be represented by a set of interconnected blocks as in figure 1 (the blocks can be the representation of transistors, gates, or even whole designs). An interconnection between blocks is called a *net*. A net that is connected to more than two blocks is called a *multi-point net*. We will assume that a net cannot have more than one connection to the same block. Some of the nets are also connected to the outside of the design. These nets are called *external nets* (as opposed to the *internal nets* which only connect blocks within the design). In order to model these external nets properly, we introduce a new kind of block which we will call a *pin*. The other blocks will be called *logic blocks*. Every external net will be connected with exactly one pin. Note that the number of pins thus equals the number of external nets. The *net degree* of a (multi-point) net will be defined as the number of blocks (logic blocks and pins) the net is connected to.

Partitioning a design means dividing this design into disjoint sub-designs (called *modules*), each containing a subset of the blocks (Fig. 2). This partitioning is done using some kind of criterion. Generally, the criterion is to minimize the number of net cuts, i.e. the number of nets crossing the borders of modules in the partition. Nets that are cut by module boundaries are shared between two or more modules and are said to be external to the modules. Therefore the net will be split into a number of sub-nets, one for each module that shares the net. A new pin will be assigned to each sub-net (if the net was already external to the design then the pin assigned to it can be reused for one of the sub-nets). Each module can then itself be seen as a design and can be partitioned further. A partitioning process where the modules themselves are recursively partitioned will be called a *hierarchical partitioning method*.

Designs can be classified on the basis of their interconnection complexity. This *interconnection complexity* of a design is based on the notion that some designs have a totally different structure of interconnections than others. These differences in interconnection complexity over all designs have been experimentally observed by Rent and his observations led to the well-known Rent's rule [5, 12].

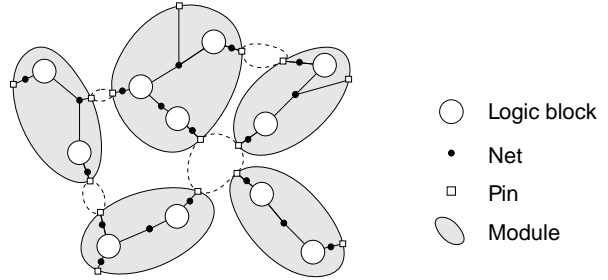


Figure 2. Partitioning the design of figure 1.

This rule is a relationship between the number of elementary blocks B in a module of a partitioned design, and the number of the module's external connections (pins) P :

$$P = FB^r, \quad (1)$$

where F is the average number of terminals per logic block, and r is called the *Rent exponent*. This exponent is a measure of the interconnection complexity of the design. Its value is bounded by 0 and 1, with increasing values for increasing interconnection complexity. Generally, r ranges from 0.47 for regular designs (such as RAMs), up to 0.75 for complex designs (such as fast full custom VLSI designs) [6]. The validity of Rent's rule is a result of the fact that designers tend to build their designs hierarchically, imposing the same complexity at each level of hierarchy. This leads to the observed "self-similarity" of designs.

3 Characterizing the behaviour of multi-point nets during the partitioning process

Partitioning a design into modules as described in section 2 involves the cutting of those nets that cross module boundaries. The questions that immediately arise are "Which interconnections will be cut?" and "How many of the interconnections will be cut at each partitioning step?" Let us first try to answer the second question.

If we take the partitioning criterion to be the minimal number of nets cut (the minimal number of pins), then the average number of pins at each level of the hierarchy can be calculated using Rent's rule [1]. Rent's rule estimates the number of pins $P(B)$ of a sub-design containing B logic blocks as (equation 1)

$$P(B) = FB^r \quad (0 < r < 1).$$

Suppose we have a total of G gates, divided into modules of size B . The total number of pins for sub-designs of size B is then given by

$$P_{tot}(B) = FB^r \frac{G}{B} = FGB^{r-1}. \quad (2)$$

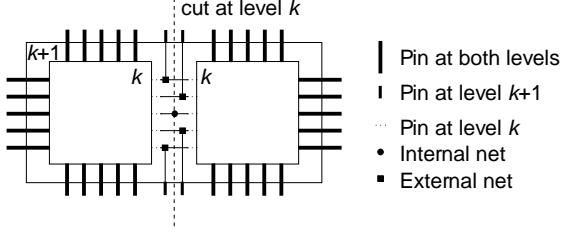


Figure 3. The number of nets cut at level k .

Let us assume that the partitioning process divides the design into two modules of equal size at each recursion level of the hierarchical partitioning. Let us number the recursion levels from $K - 1$ (for the division of the whole design into two equal modules) down to 0 (for the division at the lowest level where each module only contains 1 logic block). Then the module size B at hierarchical level k is given by 2^k and the total number of logic blocks in the design G should equal 2^K where k is the number of the recursion level in the partitioning scheme and K is the number of recursion levels ($0 \leq k \leq K - 1$). The number of pins that will be generated by the division of nets at recursion level k therefore equals

$$\begin{aligned} P_d(k) &= P_{tot}(2^k) - P_{tot}(2^{k+1}) \\ &= F 2^K 2^{k(r-1)} (1 - 2^{r-1}) \end{aligned} \quad (3)$$

In order to find the number of nets cut at level k we have to take a closer look at the division process. Consider the partitioning process at level k where a design with $F 2^{(k+1)r}$ pins is divided into two modules with $F 2^{kr}$ pins each (figure 3). The number of new pins generated by the partitioning process is given by $P_d(k)$ (equation 3). Consider the number of pins produced by the cutting of nets. An internal net at level $k + 1$ does not have any pins connected to it. After cutting the net, two new pins are generated. An external net at level $k + 1$, on the other hand, already uses a pin so only one new pin has to be generated (the other pin can be reused). With $S_i(k)$ and $S_e(k)$ the total number of internal and external nets cut at level k , this implies

$$2 S_i(k) + S_e(k) = P_d(k) \quad (4)$$

Both $S_i(k)$ and $S_e(k)$ can be zero (but not at the same time). The total number of nets cut at level k (i.e. $S_i(k) + S_e(k)$) can thus vary between $P_d(k)/2$ and $P_d(k)$ depending on what kind of nets is cut more. We will take this variation into consideration by introducing a factor $f(k)$ which represents the fraction of nets cut at level k that are internal to level $k + 1$. Thus

$$f(k) = \frac{S_i(k)}{S_i(k) + S_e(k)}. \quad (5)$$

This fraction $f(k)$ ranges between 0 and 1. Due to the self-similarity of the design at different recursion levels it is acceptable to assume that both $S_i(k)$ and $S_e(k)$ scale with k in the same way as $P_d(k)$. This means that all fractions $f(k)$ are equal

$$f(k) = f \quad (6)$$

for all k . Together with equations 4 and 5 follows

$$S_i(k) = \frac{f}{1+f} P_d(k) \quad (7)$$

$$S_e(k) = \frac{1-f}{1+f} P_d(k) \quad (8)$$

The total number of external interconnections at level k always equals the total number of pins at that level

$$N_e(k) = P_{tot}(k) = F 2^K 2^{k(r-1)}. \quad (9)$$

The number of external interconnections of the design N_e therefore equals

$$N_e = N_e(K) = F 2^K r \quad (10)$$

An internal connection at level k that is cut at level $k - 1$ is external to all levels $l < k$. Therefore the total number of internal interconnections at level k ($N_i(k)$) equals

$$N_i(k) = \sum_{l=0}^{k-1} S_i(l) \quad (11)$$

$$= \frac{f}{1+f} F 2^K \left(1 - 2^{k(r-1)}\right). \quad (12)$$

As a result from this, the total number of internal interconnections N_i of the whole design should equal

$$N_i = N_i(K) = \frac{f}{1+f} (F 2^K - F 2^{Kr}). \quad (13)$$

With $2^K = G$ and N_i the total number of nets N minus the number of external nets (which equals the number of pins P), we have

$$f = \frac{N - P}{F G - N + P - F G^r} \quad (14)$$

and, with P equalling $F G^r$,

$$f = \frac{N - F G^r}{F G - N}. \quad (15)$$

4 The net degree distribution of a design

With the value of f known from the total number of nets and the number of pins in the design (equation 14) equation 12 gives the number of internal nets at each recursion level. The number of external nets $N_e(k)$ equals the number of pins at level k (equation 9). In this section we want to identify the net degree of each of those nets. Therefore we first need some definitions.

4.1 Definitions

A *net degree distribution* is a collection of values, indicating, for each net degree n , how many nets have a net degree equalling n . The sum of these values over all net degrees equals the total number of nets. A *normalized net degree distribution* denotes, for each net degree n , the fraction of nets that have net degree n .

We will represent the net degree distribution by its moment-generating polynomial. The *generating polynomial of net degrees* is defined as the polynomial in the variable x for which the coefficients of each of the terms x^n equal the number of nets with net degree n . The generating polynomial captures the whole collection of values of the net degree distribution in one expression. Each of those values can be easily accessed by observing one term of the polynomial. Setting x to 1 in the polynomial immediately provides us with the total number of nets. Differentiating the polynomial once and then setting x to 1 gives the average net degree.

The goal of the next sub-section is to find the generating polynomial of net degrees at each level of the recursive partitioning process. The net degree distribution of the whole design is not known in general (we can only measure it for a certain design). However, we do know the net degree distribution at the lowest level ($k = 0$) since at that level all modules contain only one logic block. Then, only 2-point nets exist, connecting a terminal of a logic block to a pin of the module. For this reason we will generate the net degree distribution of the design bottom-up (by a generating process instead of a partitioning process). In section 5 we will then compare the obtained net degree distribution with measurements on benchmark circuits.

4.2 Recursive equation for the polynomials

Since the internal and external nets behave differently, we will search a generating polynomial of net degrees for internal and external nets separately. We will denote the polynomial of internal net degrees on level k as $\mathcal{D}_i(k)$, the one for external nets as $\mathcal{D}_e(k)$. Their normalized versions will be denoted as $\mathcal{E}_i(k)$ for internal nets and $\mathcal{E}_e(k)$ for external nets. These polynomials represent the probability that a net at level k has net degree n , for every n , and are defined by

$$\mathcal{E}_c(k) = \frac{\mathcal{D}_c(k)}{N_c(k)} \quad c \in \{i, e\}. \quad (16)$$

The generating process is the reverse of the partitioning process and can be modelled by combining the nets of two modules at a level k to one module at level $k + 1$ (figure 3). At level 0, two modules containing only one logic block

will be combined. At that level we know there are no internal nets within the modules. Assume we know both the internal and external net degree distributions within the modules at a level k . All nets internal to level k are not visible anymore at this point and will not be changed. All nets external to level k are only visible through their corresponding module pins. The two modules at level k can be connected by internal nets (internal to level $k + 1$) or by external nets (external to level $k + 1$) as in figure 3. Each of those nets connects one pin of the first module on level k with one pin of the second module on level k . External nets are also connected to a pin of the module at level $k + 1$. Because the two modules can be considered to be black boxes, the choice of a pin for connection should be a random process, not influenced by the net degree. Nets that are not chosen for connection remain unchanged and their pins become pins of the module at level $k + 1$. All pins at level k that are not a pin at level $k + 1$ are removed.

The net generating process described above results in the following changes for the nets at level k :

- $N_e(k + 1) - S_e(k)$ external nets at level k are left unchanged and become external nets at level $k + 1$. Their net degree remains, of course, equal. Since the choice of the nets is a random process, the normalized generating polynomial for those nets is the same as the one at level k .
- $2 S_e(k)$ external nets at level k are combined to result in $S_e(k)$ external nets at level $k + 1$. Their net degree is the sum of the net degrees of the composing nets minus one (one pin is removed). Since the choice of pins for connection is a random process the new normalized generating polynomial is the multiplication of the two normalized generating polynomials.
- $2 S_i(k)$ external nets at level k are combined to result in $S_i(k)$ internal nets at level $k + 1$. Their net degree is the sum of the net degrees of the composing nets minus two (two pins are removed).
- All internal nets at level k remain unchanged and become internal nets at level $k + 1$.

The generating process described above is reflected in the following equations between the generating polynomials:

$$\begin{aligned} \mathcal{D}_e(k + 1) &= (N_e(k + 1) - S_e(k)) \mathcal{E}_e(k) \\ &\quad + S_e(k) \frac{\mathcal{E}_e^2(k)}{x} \end{aligned} \quad (17)$$

$$\mathcal{D}_i(k + 1) = \mathcal{D}_i(k) + S_i(k) \frac{\mathcal{E}_e^2(k)}{x^2} \quad (18)$$

We know that, at level 0, there are no internal nets and only 2-point external nets (since a net cannot have more

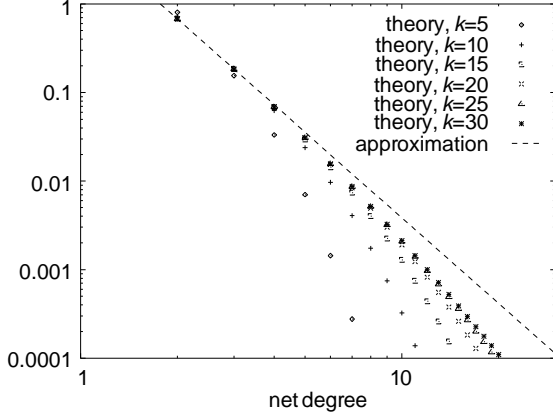


Figure 4. The internal net degree distribution for a design with Rent exponent $r = 0.6$ and fraction $f = 0.6$.

than one connection to the same logic block). This means

$$\mathcal{D}_i(0) = 0 \quad (19)$$

$$\mathcal{E}_e(0) = x^2. \quad (20)$$

Solving the recursive equations 17 and 18, together with equation 16 and the starting values given in equations 19 and 20, results in the net degree distribution at every level k . These distributions are dependent on both the Rent exponent r and the fraction f . The general solution of the recursive equations as a function of k is difficult to obtain (if not impossible). A numerical analysis for some typical value for the Rent exponent r and for the fraction f (figure 4) shows that the normalized internal net degree distribution follows approximately a power law for the first values of n (especially for large designs, $k \gg 1$) and starts to drop rapidly after a while. The figures for other values of r and f are similar [7]. For large designs, we can thus approximate the distribution by a power series (a straight line in a log-log plot). This distribution is fully characterized by two of its points. In [7] the recursive equations 17 and 18 are evaluated for $n = 2$ and $n = 3$.

We can approximate the net degree distribution at each level k by a power series of n as $d_k(n) = a_k n^{b_k}$ where a_k and b_k can be calculated from $d_k(2)$ and $d_k(3)$ as (see [7])

$$b_k = \frac{\log\left(\frac{d_k(3)}{d_k(2)}\right)}{\log\left(\frac{3}{2}\right)} \quad (21)$$

$$a_k = \frac{d_k(2)}{2^{\frac{\log\left(\frac{d_k(3)}{d_k(2)}\right)}{\log(3/2)}}} \quad (22)$$

where

$$d_k(2) = \frac{(1 - y_2^k) g(r, f, F, K)}{1 - y_2} \quad (23)$$

$$\frac{d_k(3)}{d_k(2)} = \frac{2}{y} \left(1 - \frac{(1 - y_3^k)(1 - y_2)}{(1 - y_2^k)(1 - y_3)} \right) \quad (24)$$

and

$$g(r, f, F, K) = \frac{f}{1 + f} F 2^K (1 - R(r)) \quad (25)$$

$$y = \frac{2R(r) - (1 - f)}{(1 + f)R(r)} \quad (26)$$

$$y_2 = \frac{(2R(r) - (1 - f))^2}{(1 + f)^2 R(r)} \quad (27)$$

$$y_3 = \frac{(2R(r) - (1 - f))^3}{(1 + f)^3 R^2(r)} \quad (28)$$

$$R(r) = 2^{r-1}. \quad (29)$$

This approximation is also shown in figure 4 and it seems to be valid for large designs (the larger the design, the better the approximation) and for small values of n . Since we know that, in most cases, more than 75% of the nets are 2- or 3-point nets [3] and also the remaining nets normally do not have that high a net degree, the approximation should suffice for the estimations in most cases. For large designs, the approximation can be easily obtained by taking the limit for $k \rightarrow \infty$. Equations 21 and 22 remain with $d_k(2)$ and $d_k(3)$ substituted by $d_\infty(2)$ and $d_\infty(3)$ respectively and

$$d_\infty(2) = \frac{g(r, f, F, K)}{1 - y_2} \quad (30)$$

$$\frac{d_\infty(3)}{d_\infty(2)} = \frac{2(y_2 - y_3)}{y(1 - y_3)} \quad (31)$$

5 Results

In section 3 we developed a new theory on the partitioning behaviour of multi-point nets. From the study of the reverse partitioning process (the net generating process), we found a recursive equation to represent the net degree distribution. In order to evaluate this net degree distribution, we numerically evaluated the recursive equation and compared the results with measurements on the ISCAS benchmark designs. The parameters characterizing these designs are presented in table 1. The Rent exponent of the benchmarks has been estimated by performing a partitioning with the 'ratiocut' program described in [14]. The fraction f has been estimated by using equation 14 and the measurements of the total number of nets N and the number of pins P from the benchmark data. The average number of terminals per gate F has been computed by counting all terminals and dividing the result by the number of gates G .

The second last and last columns of table 1 compare the measured average net degree \bar{n}_m with the theoretically estimated values for the average net degree \bar{n}_t for every bench-

Name	G	F	r	f	\bar{n}_m	\bar{n}_t
c432	160	3.10	0.62	0.565	2.750	2.557
c499	202	3.02	0.55	0.443	2.811	2.891
c1355nr	546	2.93	0.50	0.505	2.853	2.861
c2670nr	961	2.71	0.59	0.579	2.525	2.591
c3540nr	1620	2.72	0.57	0.609	2.683	2.582
c6288nr	2399	2.98	0.46	0.506	2.966	2.943
c7552	3512	2.75	0.55	0.567	2.681	2.700
s208.1	112	2.69	0.39	0.640	2.557	2.493
s298	133	2.94	0.42	0.527	2.941	2.801
s344	175	2.62	0.34	0.587	2.603	2.631
s382	179	2.83	0.34	0.546	2.830	2.775
s832	292	3.65	0.58	0.393	3.558	3.208
s953	424	2.82	0.68	0.645	2.807	2.394
s1196	547	2.88	0.64	0.606	2.856	2.525
s1423	731	2.69	0.38	0.601	2.662	2.640
s5378	2958	2.48	0.61	0.709	2.483	2.374
s9234.1	5808	2.41	0.53	0.722	2.407	2.372
s13207.1	8589	2.37	0.54	0.727	2.382	2.365
s15850	10369	2.37	0.54	0.737	2.380	2.343
s35932	17793	2.69	0.55	0.586	2.701	2.688
s38417	23815	2.41	0.48	0.710	2.416	2.404

Table 1. Parameters characterizing the ISCAS benchmark designs and comparison of the theoretical (\bar{n}_t) versus the measured (\bar{n}_m) average net degree.

mark design. The estimated average net degree clearly follows the measured one. The relative error stays below 5% of the actual value for most designs.

A plot of the measured internal net degree distribution against the theoretical one learns that both follow the same behaviour. It is not possible to show all the figures. We will confine ourselves to the largest benchmark of the ISCAS suite in figure 5. One can see that the theoretical net generating process as presented in section 3 really captures the behaviour of multi-point nets in the partitioning process. Also the approximation of the power law seems to estimate the net degree distribution well. In interpreting the results one should not worry too much about the fact that there seem to be too many points with high net degree compared to the theory. One must be aware of the fact that the normal number of nets with such net degrees is smaller than one. But in the real world the net is present or it is not present. There is no way of being partly there. In fact, the number of those nets should be spread out over all neighbouring net degrees which do not have a representative in the distribution.

The external net degree distribution is plotted in fig-

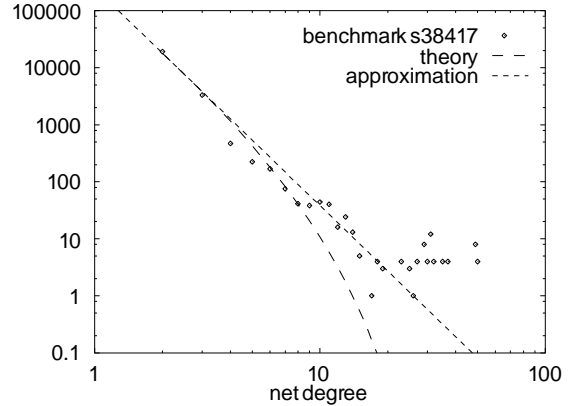


Figure 5. The measured internal net degree distribution, the theoretical estimation and a theoretical approximation for the s38417 benchmark design.

ure 6. At first sight, the theoretical distribution seems not to be as good as the internal one. However, if we look at the equations 17 and 18, we see that the internal distribution is highly dependent on the external distributions of all previous levels. If the external distribution would not be modelled correctly, the results for the internal distribution would be bad too. The reason for the big differences between theory and experiment in some of the external distributions lies in the fact that designers tend to change the external nets at the highest level in order to cope with the pin limitation problem. This is the same reason why Rent's rule does not hold at the highest level in most cases (see second region in Rent's rule [5, 12]). The ISCAS89 benchmark s38417, for instance, only has 2-point external nets at the highest level (figure 6). However, once we start partitioning the design, we begin to recognize the theoretically estimated net degree distribution almost immediately. Figure 7 shows the external net degree distribution for a partition of the benchmark design (partitioned using the 'ratio-cut' partitioning program [14]). It is clear from this figure that the big difference between the theoretical and experimental net degree distributions only resides at the highest level(s).

6 Conclusion

In this paper, we presented a new theoretical model to capture the behaviour of multi-point nets during the partitioning process. This model is able to estimate the net degree distribution accurately. To our knowledge, it is the first attempt to characterize multi-point nets in such a way. This model opens new perspectives for estimating design parameters such as interconnection lengths, area requirements, channel densities, power usage, ...

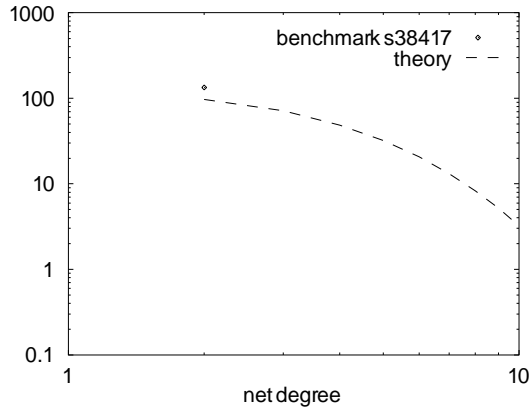


Figure 6. The measured external net degree distribution and the theoretical estimation for the s38417 benchmark design.

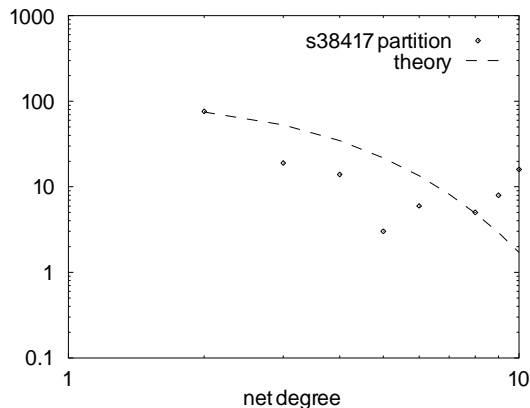


Figure 7. The measured external net degree distribution and the theoretical estimation for a partition of the s38417 benchmark design.

Further research is planned to estimate interconnection lengths for multi-point nets based on this theory. These interconnection length estimations should be superior to all previous estimations since, for the first time, multi-point nets are modelled adequately.

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References

- [1] W. E. Donath. Placement and average interconnection lengths of computer logic. *IEEE Trans. Circuits & Syst.*, vol. CAS-26: pages 272–277, 1979.
- [2] L. Hagen, A. B. Kahng, F. J. Kurdahi, and C. Ramachandran. On the intrinsic Rent parameter and spectra-based partitioning methodologies. *IEEE Trans. on Comput.-Aided Des., Integrated Circuits & Syst.*, vol. 13 (no. 1): pages 27–37, January 1994.
- [3] E. S. Kuh and T. Ohtsuki. Recent advances in VLSI layout. *Proc. of the IEEE*, vol. 78: pages 237–263, 1990.
- [4] F. J. Kurdahi and A. C. Parker. Techniques for area estimation of VLSI layouts. *IEEE Trans. Comput.-Aided Des., Integrated Circuits & Syst.*, vol. 8: pages 81–92, 1989.
- [5] B. S. Landman and R. L. Russo. On a pin versus block relationship for partitions of logic graphs. *IEEE Trans. on Comput.*, vol. C-20: pages 1469–1479, 1971.
- [6] R. L. Russo. On the tradeoff between logic performance and circuit-to-pin ratio for LSI. *IEEE Trans. Comput.*, vol. C-21: pages 147–153, 1972.
- [7] D. Stroobandt and F. J. Kurdahi. On the characterization of multi-terminal nets in computer systems. Technical report, Universiteit Gent (Vakgroep ELIS), October 1997. ELIS Tech. report DG 97-07.
- [8] D. Stroobandt and J. Van Campenhout. Estimating interconnection lengths in three-dimensional computer systems. *IEICE Trans. on Inf. & Syst., Special Issue on Synthesis and Verification of Hardware Design*, vol. E80-D (no. 10): pages 1024–1031, October 1997.
- [9] D. Stroobandt, H. Van Marck, and J. Van Campenhout. An accurate interconnection length estimation for computer logic. In *Proc. 6th Great Lakes Symp. on VLSI*, pages 50–55. IEEE Computer Society Press, March 1996.
- [10] D. Stroobandt, H. Van Marck, and J. Van Campenhout. Estimating logic cell to I/O pad lengths in computer systems. In T. Sasao, editor, *Proc. Workshop on Synthesis and System Integration of Mixed Technologies, SASIMI'97*, pages 192–198. S. Insatsu, Osaka, Japan, December 1997.
- [11] H. Van Marck, D. Stroobandt, and J. Van Campenhout. Interconnection length distributions in 3-dimensional anisotropic systems. In M. H. Hamza, editor, *Proc. 13th IASTED Intl. Conf. on APPLIED INFORMATICS*, pages 98–101. IASTED-ACTA Press, 1995.
- [12] H. Van Marck, D. Stroobandt, and J. Van Campenhout. Towards an extension of Rent's rule for describing local variations in interconnection complexity. In S. Bai, J. Fan, and X. Li, editors, *Proc. 4th Intl. Conf. for Young Computer Scientists*, pages 136–141. Peking University Press, 1995.
- [13] H. Van Marck and J. Van Campenhout. Modeling and evaluating optoelectronic architectures. In R. T. Chen and J. A. Neff, editors, *Optoelectronics II*, volume 2153 of *SPIE Proc. Series*, pages 307–314, SPIE, 1994.
- [14] Y.-C. Wei and C.-K. Cheng. Ratio cut partitioning for hierarchical designs. *IEEE Trans. Comput.-Aided Des., Integrated Circuits & Syst.*, vol. 10 (no. 7): pages 911–921, July 1991.