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Estimating interconnection lengths in three-dimensional computer systems**

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SUMMARY In computer hardware there is a constant evolution towards smaller transistor sizes. At the same time, more and more transistors are placed on one chip. Both trends make the pin limitation problem worse. Scaling down chip sizes adds to the shortage of available pins while increasing the number of transistors per chip imposes a higher need for chip terminals. The use of three-dimensional systems would alleviate this pin limitation problem. In order to decide whether the benefits of such systems balance the higher processing costs, one must be able to characterize these benefits accurately. This can be done by estimating important layout properties of electronic designs, such as space requirements and interconnection length values. For a two-dimensional placement, Donath found an upper bound for the average interconnection length that follows the trends of experimentally obtained average lengths [1]. Yet, this upper bound deviates from the experimentally obtained value by a factor of approximately 2 which is not sufficiently accurate for some applications. In this paper, we first extend Donath's technique to a three-dimensional placement. We then compute a significantly more accurate estimate by taking into account the inherent features of the optimal placement process.

key words: three-dimensional systems, interconnection length, Rent's rule, Donath's hierarchical placement technique, global interconnection length distribution.

1. Introduction

Creating a physical layout of an electronic design involves the placement and interconnection of elementary blocks onto a carrier. Important properties of such layouts are area (or space) requirements and interconnection lengths. The ability to predict these properties, without actually having to perform the placement and routing itself, is important for the following reasons:

- Most placement algorithms use estimates for interconnection lengths and area requirements to limit the search in the solution space [2].
- The predictions offer a way to gain a more fundamental insight in the placement of designs on different carriers [3].

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There have been many attempts to predict area requirements and interconnection lengths. A first upper bound for interconnection lengths has been found by Sutherland and Oestreicher [4]. Since it is based on a random placement, it yields excessively large estimates. Donath [1] found that a hierarchical placement technique gives much better interconnection length estimates and his results have been used by several other researchers [5], [6]. Recently, we have extended Donath's technique to include knowledge about an optimal placement process [7]–[9]. This resulted in a significant improvement of the interconnection length estimation for designs placed in a two-dimensional system.

Chip sizes are scaled down rapidly and the number of transistors per chip increases likewise. The first evolution leads to a smaller available pin count since the perimeter of the chip decreases while the I/O-pad size remains equal. The second one, on the other hand, imposes a much higher need for chip terminals to provide the necessary communication with other components. This leads to highly pin limited designs. The problem can be alleviated by using three-dimensional systems, creating more nearest neighbours to every node. Such systems should closely relate to a three-dimensional mesh in order to have a much more dense interconnection structure than is possible in the fundamentally two-dimensional (backplane) systems we know today. Current research more and more evolves towards the implementation of designs in such three-dimensional systems [10]–[12]. It is not yet clear what these systems should look like and how they should be implemented (totally electronic or partially optical?). Therefore, a theoretical estimation of the most important features for such systems is badly needed. Accurate estimates can verify the usefulness of a proposed architecture before it is actually built. These estimates can also be used to choose the technology in which to implement the third dimension. For this to be possible, Donath's technique should be extended to three dimensions. This will be the topic of Sect. 2 and Sect. 3. In Sect. 4, we will improve the method by taking into account more knowledge about an optimal placement process. As a result, we will compare the new estimates with those obtained by simply extending Donath's technique to three dimensions and with the estimates for a two-dimensional implementation.

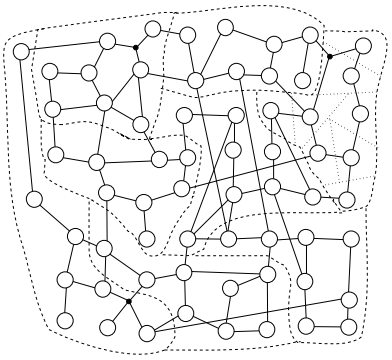

Fig. 1 Recursive partitioning scheme of the design.

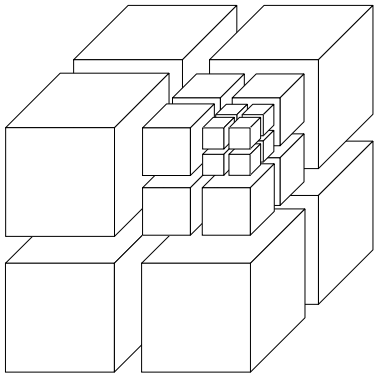

Fig. 2 Recursive partitioning scheme of the architecture.

2. Donath's Technique in Three Dimensions

Donath estimates the average interconnection length using three models [1]: one for the design itself, one for the architecture the design will be placed in and a third model for the placement process.

The design is characterized by its interconnection complexity which can be modelled using a relationship between the number of logic gates B in a module of a partitioned design, and the number of the module's terminals T, known as Rent's rule [13]:

$$T = FB^r, \tag{1}$$

where F is the average number of interconnections per logic gate (fanin & fanout), and r is called the Rent exponent. This exponent is a measure of the interconnection complexity of the design. Its value is bounded by 0 and 1, with increasing values for increasing interconnection complexity. Generally, r ranges from 0.47 for regular designs (such as RAM), up to 0.75 for complex designs (such as fast full custom VLSI designs) [14]. Rent's rule holds for a wide range of designs due to the fact that designers tend to build their designs hierarchically, imposing the same complexity on the design at each level of hierarchy.

In this paper, we extend Donath's technique to three-dimensional architectures, which can be modelled as a cubic Manhattan grid [9]. In this grid, each grid point (or *cell*) corresponds to a location where one logic gate of the design can be placed. The grid lines correspond to the *channels* in which the connections between the gates can be routed. All lengths are measured using a Manhattan metric.

Donath's theoretical partitioning and placement scheme is based on a hierarchical placement of the design into the physical architecture [1]. We define an *optimal placement* as one that minimizes the total interconnection length. This optimal placement should be correctly modelled by the hierarchical placement method. In this method, the design and the architecture are partitioned hierarchically into sub-designs and sub-architectures. Due to the cubic symmetry of the architecture, each step in the partitioning hierarchy divides the design and the architecture into eight sub-parts (instead of four as in [1]). Each sub-design (sub-architecture) at a hierarchical level consists itself of eight sub-designs (sub-architectures) of equal size at the next (lower) level of hierarchy (Fig. 1 and Fig. 2). We thus assume that the number of gates in the logic design is a power of 8 (there are 8^K gates, with K the number of hierarchical levels). Each sub-design is paired with a sub-architecture until all gates are paired with (and essentially assigned to) exactly one cell. The recursion levels will be numbered $K-1$ (eight sub-designs that constitute the whole design) down to 0 (eight sub-designs consisting of only one logic gate).

The partitioning of the design into eight sub-designs of equal size should be done in such a way that the partition satisfies Rent's rule. That is, we want to keep the number of interconnections between the sub-designs as low as possible. This ensures that our placement scheme is a good model for the optimal placement of the design. It is indeed obvious that, in an optimal placement, densely interconnected logic gates are placed as close as possible, resulting in clusters of such gates. Among clusters, there are fewer interconnections. This behaviour is modelled accurately by Rent's rule.

Given the above model for the design, the physical architecture and the placement technique, we want to find the average interconnection length. We shall do this by calculating the average number of interconnections $\bar{n}_k$ and the average length of the interconnections $\bar{l}_k$ at every hierarchical level k ($0 \leq k \leq K-1$). The average interconnection length $\mathcal{L}$, computed over all hierarchical levels, is then given by

$$\mathcal{L} = \frac{\sum_{k=0}^{K-1} \bar{n}_k \bar{l}_k}{\sum_{k=0}^{K-1} \bar{n}_k}. \tag{2}$$

3. The Average Interconnection Length

The expected number of interconnections at each hierarchical level can be calculated using Rent's rule (Eq. 1):

$$T = FB^r \qquad (0 < r < 1).$$

Suppose we have a total of G gates, divided into clusters of size B. The total number of terminals for all sub-designs of size B is then given by

$$T_{tot}(B) = FB^r \frac{G}{B} = FGB^{r-1}.$$

For three-dimensional partitioning, $B = 8^k$ and $G = 8^K$ where k is the recursion level in the partitioning scheme and K is the number of recursion levels ($0 \leqq k \leqq K-1$). The number of terminals T_k belonging to recursion level k is given by

$$T_k = T_{tot}(8^k) - T_{tot}(8^{k+1}). \tag{3}$$

Note that terminals of sub-designs of size $8^{(k+1)}$ are also terminals of sub-designs of size 8^k. This means that $T_{tot}(8^k)$ includes all terminals of sub-designs of size $8^{(k+1)}$. Equation 3 expresses the fact that these higher level terminals are external to level k and hence should be subtracted from $T_{tot}(8^k)$.

The expected number of interconnections (nets) at each level of the hierarchy ($\bar{n}_k$) is a fraction α of the number of terminals T_k. The value of α is $1/2$ if each net has just two terminals, and somewhat smaller in the normal case where there are some multi-terminal nets. Since the range of variation is relatively small for α, it is a good approximation to assume that variations of α are insignificant [1]. We then have

$$\bar{n}_k = \alpha T_k = \alpha\, F\, 8^K \left(1 - 8^{r-1}\right) 8^{k(r-1)}. \tag{4}$$

We next determine the average interconnection length $\bar{l}_k$ at hierarchical level k. The interconnections belonging to hierarchical level k are those interconnections between gates belonging to the same $(k+1)$-th level sub-design, but to different k-th level sub-designs. Those interconnections connect two gates placed in different cubes at hierarchical level k. Three different combination classes are possible: either the cubes are adjacent (A) or they are diagonally opposed to a nearby (N) location or they are diagonally opposed to a remote (R) location (Fig. 3). We will call a combination of the first class an A-*combination*, of the second one an N-*combination*, and of the last one an R-*combination*.† For each of these combinations, we compute the average interconnection length (denoted as $\bar{l}_{k,a}$, $\bar{l}_{k,n}$, and $\bar{l}_{k,r}$ respectively). It is assumed that the starting points and the endpoints of the interconnections between two cubes are uniformly distributed over those cubes and that every point in one cube can be interconnected with any point in the other cube.

†There are twelve A-combinations, twelve N-combinations and four R-combinations in a cube.

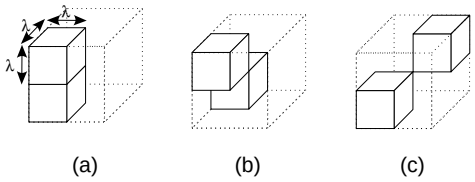

Fig. 3 Three possible combination classes at a hierarchical level k: A-combinations (a), N-combinations (b), and R-combinations (c). All cubes have size $\lambda^3 = 8^k$.

In the remaining of this paper, we define an *interconnection length distribution* as a collection of values, indicating, for each length l, how many interconnections have length l. The sum of these values over all lengths l equals the total number of interconnections. A *normalized interconnection length distribution* denotes, for each length l, the fraction of interconnections that has length l.

The normalized interconnection length distributions can be calculated as in [6] but for the three-dimensional cubic combinations. These distributions are denoted as $P_{k,a}(l)$ for A-combinations, $P_{k,n}(l)$ for N-combinations and $P_{k,r}(l)$ for R-combinations. A much more elegant way to compute these distributions is based on generating polynomials [15] and is presented in [8]. The resulting distributions are displayed here without proof for combinations of cubes with side $\lambda = 2^k$. Note that, inside a cube, the largest distance in one dimension equals $\lambda - 1$.

$$P_{k,a}(l) = \begin{cases} \frac{1}{30\lambda^6} P^i_{k,a}(l) & i\lambda \leqq l < (i+1)\lambda, \\ & \text{where } i = 0, \ldots, 3 \\ 0 & \text{otherwise,} \end{cases} \tag{5}$$

with

$$\begin{aligned} P^0_{k,a}(l) &= \left(20\,l^3 + 10\,l\right)\lambda^2 + \left(10\,l^2 - 10\,l^4\right)\lambda \\ &\quad + l^5 - 5\,l^3 + 4\,l, \\ P^1_{k,a}(l) &= 74\,\lambda^5 - 260\,l\,\lambda^4 + \left(340\,l^2 - 30\right)\lambda^3 \\ &\quad + \left(110\,l - 180\,l^3\right)\lambda^2 - 3\,l^5 + 15\,l^3 - 12\,l \\ &\quad + \left(40\,l^4 - 80\,l^2 + 16\right)\lambda, \\ P^2_{k,a}(l) &= -758\,\lambda^5 + 1420\,l\,\lambda^4 - \left(980\,l^2 - 310\right)\lambda^3 \\ &\quad - \left(360\,l - 320\,l^3\right)\lambda^2 + 3\,l^5 - 15\,l^3 \\ &\quad - \left(50\,l^4 - 130\,l^2 + 32\right)\lambda + 12\,l, \\ P^3_{k,a}(l) &= \prod_{j=-2}^{2} (4\,\lambda - l + j) \end{aligned}$$

for an A-combination,

$$P_{k,n}(l) = \begin{cases} \frac{1}{60\lambda^6} P^i_{k,n}(l) & i\lambda \leqq l < (i+1)\lambda, \\ & \text{where } i = 0, \ldots, 4 \\ 0 & \text{otherwise,} \end{cases} \tag{6}$$

with

$$P^0_{k,n}(l) = \left(5\,l^4 - 5\,l^2\right)\lambda - l^5 + 5\,l^3 - 4\,l,$$

$$
\begin{aligned}
P^1_{k,n}(l) =& -25\,\lambda^5 + 105\,l\,\lambda^4 - \left(170\,l^2 - 45\right)\lambda^3 \\
&- \left(115\,l - 130\,l^3\right)\lambda^2 + 4\,l^5 - 20\,l^3 + 16\,l \\
&- \left(40\,l^4 - 90\,l^2 + 20\right)\lambda, \\
P^2_{k,n}(l) =& \,775\,\lambda^5 - 1655\,l\,\lambda^4 + \left(1350\,l^2 - 475\right)\lambda^3 \\
&+ \left(605\,l - 510\,l^3\right)\lambda^2 - 6\,l^5 + 30\,l^3 \\
&+ \left(90\,l^4 - 240\,l^2 + 60\right)\lambda - 24\,l, \\
P^3_{k,n}(l) =& -3275\,\lambda^5 + 4555\,l\,\lambda^4 - \left(865\,l - 630\,l^3\right)\lambda^2 \\
&- \left(2430\,l^2 - 1055\right)\lambda^3 + 4\,l^5 - 20\,l^3 \\
&- \left(80\,l^4 - 230\,l^2 + 60\right)\lambda + 16\,l, \\
P^4_{k,n}(l) =& \prod_{j=-2}^{2} (5\,\lambda - l + j)
\end{aligned}
$$

for an N-combination, and

$$
P_{k,r}(l) = \begin{cases} \frac{1}{120\lambda^6} P^i_{k,r}(l) & i\lambda \leqq l < (i+1)\lambda, \\ & \text{where } i = 0, \ldots, 5 \\ 0 & \text{otherwise,} \end{cases} \tag{7}
$$

with

$$
\begin{aligned}
P^0_{k,r}(l) =& \,l^5 - 5\,l^3 + 4\,l, \\
P^1_{k,r}(l) =& \,6\,\lambda^5 - 30\,l\,\lambda^4 + \left(60\,l^2 - 30\right)\lambda^3 \\
&+ \left(90\,l - 60\,l^3\right)\lambda^2 + \left(30\,l^4 - 90\,l^2 + 24\right)\lambda \\
&- 5\,l^5 + 25\,l^3 - 20\,l, \\
P^2_{k,r}(l) =& -474\,\lambda^5 + 1170\,l\,\lambda^4 - \left(1040\,l^2 - 570\right)\lambda^3 \\
&- \left(810\,l - 540\,l^3\right)\lambda^2 + 10\,l^5 - 50\,l^3 \\
&- \left(120\,l^4 - 360\,l^2 + 96\right)\lambda + 40\,l, \\
P^3_{k,r}(l) =& \,4386\,\lambda^5 - 6930\,l\,\lambda^4 + \left(4260\,l^2 - 2130\right)\lambda^3 \\
&+ \left(1890\,l - 1260\,l^3\right)\lambda^2 - 10\,l^5 + 50\,l^3 \\
&+ \left(180\,l^4 - 540\,l^2 + 144\right)\lambda - 40\,l, \\
P^4_{k,r}(l) =& -10974\,\lambda^5 + 5\,l^5 - \left(5340\,l^2 - 2670\right)\lambda^3 \\
&+ 12270\,l\,\lambda^4 - \left(1710\,l - 1140\,l^3\right)\lambda^2 \\
&- \left(120\,l^4 - 360\,l^2 + 96\right)\lambda - 25\,l^3 + 20\,l, \\
P^5_{k,r}(l) =& \prod_{j=-2}^{2} (6\,\lambda - l + j)
\end{aligned}
$$

for an R-combination.

One can convince oneself of the plausibility of these expressions by considering a few extreme (simple) cases, e.g.

$$
\begin{aligned}
l = 1 &\Rightarrow P_{k,a}(1) = \frac{\lambda^2}{\lambda^6}, P_{k,n}(1) = P_{k,r}(1) = 0; \\
l = 2 &\Rightarrow P_{k,n}(2) = \frac{\lambda}{\lambda^6}, P_{k,r}(2) = 0; \\
l = 3 &\Rightarrow P_{k,r}(3) = \frac{1}{\lambda^6}; \\
l = 4\,\lambda - 3 &\Rightarrow P_{k,a}(4\,\lambda - 3) = \frac{4}{\lambda^6}; \\
l = 5\,\lambda - 3 &\Rightarrow P_{k,r}(5\,\lambda - 3) = \frac{2}{\lambda^6}; \\
l = 6\,\lambda - 3 &\Rightarrow P_{k,r}(6\,\lambda - 3) = \frac{1}{\lambda^6}.
\end{aligned}
$$

The average interconnection length for each combination of level k is now found as $\bar{l}_{k,C}$ $(C \in \{a, n, r\})$

$$
\bar{l}_{k,C} = \frac{\sum_{l=0}^{6\lambda} l P_{k,C}(l)}{\sum_{l=0}^{6\lambda} P_{k,C}(l)}. \tag{8}
$$

We obtain

$$
\bar{l}_{k,a} = \frac{5\lambda}{3} - \frac{2}{3\lambda}, \quad \bar{l}_{k,n} = \frac{7\lambda}{3} - \frac{1}{3\lambda}, \quad \bar{l}_{k,r} = 3\lambda,
$$

with $\lambda = 2^k$.

Since there are twelve A-, twelve N-, and four R-combinations, the total average interconnection length $\bar{l}_k$ at the hierarchical level k is given by

$$
\bar{l}_k = \frac{12\,\bar{l}_{k,a} + 12\,\bar{l}_{k,n} + 4\,\bar{l}_{k,r}}{28} \tag{9}
$$

$$
= \frac{15\lambda}{7} - \frac{3}{7\lambda}. \tag{10}
$$

Combining Eq. 2, 4, and 10 yields

$$
\mathcal{L} = \frac{15\,H(K,r,2) - 3\,H(K,r,4)}{7\,H(K,r,3)}, \tag{11}
$$

with

$$
H(K,r,x) = \frac{2^{K(3r-x)} - 1}{2^{3r-x} - 1}. \tag{12}
$$

Note that this function should be extended continuously in the singular point $r = x/3$.

4. Refining upon the Length Estimates

4.1 Evaluation

The estimating technique presented in the previous section is primarily based on the hierarchical placement scheme. Every hierarchical level is treated separately without any knowledge about the length of interconnections from other levels of hierarchy. Up to now, it is simply assumed that the starting points of interconnections belonging to a level k, are uniformly distributed over the cells of the cubic grid on that level. It is nevertheless clear that an optimal placement strategy will place interconnected logic gates as close as possible, regardless of the hierarchical level the interconnection belongs to. This means that an optimal placement procedure will place gates that are interconnected to a gate of another cube (at level k) preferably near the border of the

two cubes. Note that, since the average number of interconnections per gate is a constant (F), the placement of interconnected gates near the border of the cubes at level k forces the interconnections at lower levels (e.g. $k-1$) to the center of the cube at level k which is, again, the border of a cube at level $k-1$. This clearly represents the optimal placement behaviour. The interconnection length estimates of Sect. 3 do not take full account of this information that is inherent to an optimal placement.

4.2 Structural and Occupancy Distributions

By assuming that all gates are connected to all other gates at one hierarchical level, one obtains an interconnection length distribution depending only on the physical architecture the design will be placed in. We will call this the *structural distribution*. The distributions $P_{k,a}$, $P_{k,n}$, and $P_{k,r}$ that we calculated in Sect. 3 are structural distributions for the cubic Manhattan grid. We can also assign to each length the probability that the interconnection corresponding with that length would be laid out in a real placement procedure and with a real design with the specified Rent exponent. This leads to an *occupancy distribution*.

Each interconnection length distribution can be factorized as the product of the structural distribution and the occupancy distribution. The assumption of a uniform distribution of interconnection starting points leads to a uniform occupancy distribution at each hierarchical level. The interconnection length is then only depending on the structural distribution at that level. This, in fact, is the main reason for the overestimation of interconnection lengths in [1]. We shall introduce a non-uniform occupancy distribution, following the intuitive notion that an optimal placement process would place interconnected gates at cells close to each other. Therefore, the occupancy distribution should decrease with increasing length. It is obvious that the occupancy distribution should also depend on the design complexity (Rent exponent) since it is harder, even for an optimal placement process, to place complex designs than it is to place simple designs.

4.3 The Global Interconnection Length Distribution

In [16], simple theoretical considerations are used to indicate that the normalized distribution $f_{2D}(l)$ of interconnection lengths for a good two-dimensional placement in a square Manhattan grid should be of the form

$$\begin{array}{lll} f_{2D}(l) & \approx & g l^{2r-3} \quad (1 \leqq l \leqq L) \\ & \approx & 0 \qquad\quad (l > L). \end{array} \tag{13}$$

In this distribution g is a normalization constant, L is a constant related to the size of the square grid, and r is the Rent exponent. The distribution $f_{2D}(l)$ will be called the *global distribution* and can be defined as

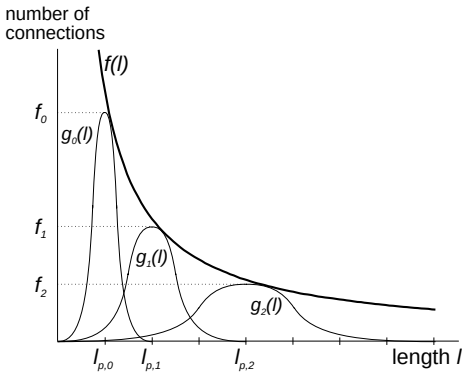

Fig. 4 Local distributions contribute to the global distribution $f(l)$. Only the first three local distributions are shown and for clarity distributions are shown as continuous ones.

the interconnection length distribution of the whole design. It contains information about all interconnections together. At each hierarchical level, we can also define a *local distribution*. Such a distribution only contains information about interconnections at a specified hierarchical level.

In [7], it is shown that the trend of $f_{2D}(l)$ (Eq. 13) mainly depends on the number of interconnections $\bar{n}_k$ at hierarchical level k and not on the way these interconnections are distributed locally. We will now show that the same applies to a three-dimensional placement, resulting in an equation, similar to Eq. 13. Consider the local distribution $g_k(l)$ of interconnection lengths at hierarchical level k ($g_k(l) = 0$ for $l > 6\,2^k$) and assume, for clarity, that these are continuous distributions. Due to Rent's rule, which is a result of the self-similarity within designs, the interconnection complexity is similar at all hierarchical levels k. This leads us to the assumption that the local distributions $g_k(l)$ have similar shapes. Now, consider the peak value f_k of $g_k(l)$ and the length $l_{p,k}$ for which $f_k = g_k(l)$. Due to the similar shapes of all $g_k(l)$, $l_{p,k}$ scales with 2^k (Fig. 4). We assume that the peak of the distributions $g_k(l)$ is sufficiently sharp so that every $g_k(l)$ contributes to the global distribution $f(l)$ ($= \sum_{k=0}^{K-1} g_k(l)$) mainly around $l_{p,k}$. The global distribution $f(l)$ will then be determined by the values f_k. Since the total number of interconnections at hierarchical level k equals $\bar{n}_k$, we have

$$\int g_k(l)dl = \bar{n}_k \qquad (0 \leqq k \leqq K-1).$$

The integral is proportional to the product of the peak value f_k and the length of the support of $g_k(l)$ by a factor A. Because we assume that all $g_k(l)$ have similar shapes, this factor is the same for all k and

$$f_k\, 6\, 2^k = A\, \bar{n}_k$$

for all $k, 0 \leqq k \leqq K-1$. Using the value of $\bar{n}_k$ (Eq. 4) this yields

$$f_k = f_0\, 2^{k(3r-4)},$$

and, since the values of $l_{p,k}$ scale with 2^k,

$$f(l) \sim l^{3r-4}. \tag{14}$$

These simple considerations show that the trend of the distribution $f(l)$ (Eq. 14) only depends on the scaling behaviour of the local distributions $g_k(l)$ and not on the distributions themselves. Because the structure of the cubic grid can only have a minor impact on the global distribution found in Eq. 14 (especially for very large designs), this distribution can be seen as the occupancy distribution of the whole design. The scalability of designs that obey Rent's rule indicates that the occupancy distribution should not depend on the size of the design, nor on the part of the design that we are looking at. On average, the length distribution of interconnections starting from any cell should follow Eq. 14. This equation can therefore be used as the occupancy distribution at each hierarchical level.

4.4 Mathematical Derivation of the Average Interconnection Length

We multiply the structural distributions $P_{k,C}(l)$ ($C \in \{a,n,r\}$) with the non-uniform occupancy distribution $f(l)$, given by Eq. 14, to obtain the local distributions. Therefore Eq. 8 becomes

$$\bar{l}_{k,C} = \frac{\sum_{l=0}^{6\lambda} l P_{k,C}(l) f(l)}{\sum_{l=0}^{6\lambda} P_{k,C}(l) f(l)} = \frac{\sum_{l=0}^{6\lambda} P_{k,C}(l) l^{3r-3}}{\sum_{l=0}^{6\lambda} P_{k,C}(l) l^{3r-4}}. \tag{15}$$

The sums in Eq. 15 can not be computed analytically without knowing the value for $\lambda = 2^k$. Yet, if we want to compare our new results with those found in Sect. 3, both numerically and theoretically, an analytical form of the average interconnection length is needed. A way around this problem is to approximate the discrete distributions by continuous ones. One can easily verify that the continuous form of Eq. 5 through 7 is found by removing all terms for which the sum of the degrees in l and λ is less than 5. These terms correspond to boundary effects which disappear in the continuous case. The continuous forms $P^c_{k,a}(l)$, $P^c_{k,n}(l)$, and $P^c_{k,r}(l)$ of $P_{k,a}(l)$, $P_{k,n}(l)$, and $P_{k,r}(l)$ respectively are given in detail in [8] and [9].

A substitution of the sums in Eq. 15 by integrals, yields

$$\bar{l}_{k,C} = \frac{\int_0^{6\lambda} P^c_{k,C}(l) l^{3r-3} dl}{\int_0^{6\lambda} P^c_{k,C}(l) l^{3r-4} dl}.$$

This results in $\bar{l}_{k,C} = \lambda R_C(r)$, $C \in \{a,n,r\}$ with

$$R_C(r) = \frac{(r-1)}{(r+1)} \frac{T_C(r)}{N_C(r)},$$

and

$$\begin{aligned}
T_a(r) &= 4^{3r+3} - 2(r+3)3^{3r+3} \\
&\quad + (9r^2 + 51r + 66)2^{3r+1} \\
&\quad - 2(9r^2 + 24r + 17) \\
N_a(r) &= 4^{3r+2} - 2(3r+8)3^{3r+1} \\
&\quad + (9r^2 + 45r + 50)2^{3r} \\
&\quad - 2(9r^2 + 18r + 10), \\
T_n(r) &= 5^{3r+3} - (3r+23)4^{3r+2} + 12r + 17 \\
&\quad + 2(2r+7)3^{3r+3} - (9r+19)2^{3r+3}, \\
N_n(r) &= 5^{3r+2} - (3r+22)4^{3r+1} + 12r + 13 \\
&\quad + 2(6r+19)3^{3r+1} - (9r+16)2^{3r+2}, \\
T_r(r) &= 6^{3r+2} - 5^{3r+3} + 10\,4^{3r+2} - 10\,3^{3r+2} \\
&\quad + 5\,2^{3r+2} - 1, \\
N_r(r) &= 6^{3r+1} - 5^{3r+2} + 10\,4^{3r+1} - 10\,3^{3r+1} \\
&\quad + 5\,2^{3r+1} - 1.
\end{aligned}$$

Using Eq. 9, this results in

$$\bar{l}_k = \lambda R(r),$$

with

$$R(r) = \frac{12R_a(r) + 12R_n(r) + 4R_r(r)}{28}. \tag{16}$$

The sum over all hierarchical levels (Eq. 2) then yields

$$\mathcal{L} = R(r) \frac{H(K,r,2)}{H(K,r,3)}, \tag{17}$$

with $H(K,r,x)$ given by Eq. 12

$$H(K,r,x) = \frac{2^{K(3r-x)} - 1}{2^{3r-x} - 1}.$$

5. Results

The average interconnection length based on the non-uniform occupancy distribution (Eq. 17) has the same scaling behaviour[†] as the average interconnection length based on the uniform occupancy distribution (Eq. 11). This is a necessary consequence of the fact that we used the same hierarchical placement technique with the number of interconnections at every hierarchical level estimated by Rent's rule. However, the multiplication factor $R(r)$ in Eq. 17 is smaller than the factor $15/7$ found in Eq. 11, for all possible values of r (Fig. 5). Unlike this constant factor, the factor $R(r)$ increases with increasing r, corresponding to the fact that more complex designs (with a higher Rent exponent r) tend to have longer interconnections. Note that this effect is supplementary to the scaling behaviour in the factor

[†]This means that they have the same behaviour if the number of hierarchical levels increases to infinity ($K \to \infty$, i.e. the number of gates $G = 8^K$ increases to infinity).

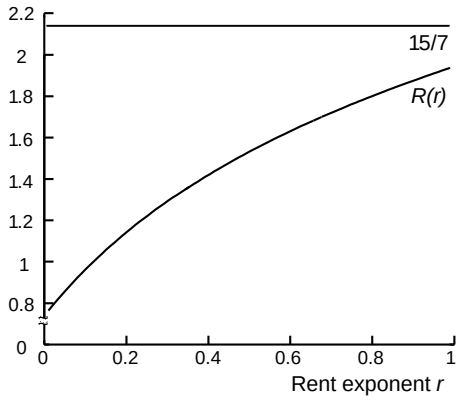

Fig. 5 $R(r)$ (Eq. 16) versus the constant factor $^{15}/_{7}$ (Eq. 11).

$$H(K,r) = \frac{H(K,r,2)}{H(K,r,3)}. \tag{18}$$

For complex designs, the scaling factor $H(K,r)$ is high because there are relatively more interconnections at higher levels of the hierarchy (and thus with higher length) than is the case with designs of low complexity. This can be seen in the equation for $\bar{n}_k$ (Eq. 4). The factor $R(r)$, on the other hand, increases with r because, for complex designs, it is difficult to place all logic gates connected to the outside of a cube on a hierarchical level, close to the border of that cube. For designs with a low Rent exponent, nearly all such gates can be placed near the border. The usage of a uniform occupancy distribution describes the case where the placement program can not decide where to place the gates. Therefore, the average interconnection length values based on Eq. 11 are overestimated, especially for designs with low complexity. In all cases ($0 < r < 1$) our new estimate of the average interconnection length is more accurate than the one found by assuming a uniform occupancy distribution.

In order to verify our average length estimations, we compared the two methods for the benchmark designs used in [7]. Therefore, we set up some experiments. The benchmark designs were placed in a two-dimensional Manhattan grid using *Simulated Annealing* [17]. Our simulated annealing program searches for the placement resulting in the lowest total interconnection length. The resulting experimental placements are therefore good samples of the optimal placement. The results are shown in Table 1. In this table, $\mathcal{L}_{exp}^{2D}$ denotes the experimentally measured value of the average interconnection length for a two-dimensional placement. The theoretical values found by using a non-uniform occupancy distribution are denoted as $\mathcal{L}_N^{xD}$ and those found by using a uniform occupancy distribution by $\mathcal{L}_U^{xD}$. They are shown both for the two- and three-dimensional case ($x = 2$ or $x = 3$). One can see that the new estimates are much lower than the first ones in both dimensions.

Table 1 Average interconnection lengths of some benchmark designs based on a non-uniform ($\mathcal{L}_N$) versus a uniform ($\mathcal{L}_U$) occupancy distribution, in two and three dimensions. The number of gates is shown in the column N_g and r is the Rent exponent. The circuits numbered 1 through 5 are those used by Donath in [1], the others are the same as those used in [7].

No.	N_g	r	$\mathcal{L}_{exp}^{2D}$	$\mathcal{L}_U^{2D}$	$\mathcal{L}_N^{2D}$	$\mathcal{L}_U^{3D}$	$\mathcal{L}_N^{3D}$	$\frac{\mathcal{L}_U^{3D}}{\mathcal{L}_U^{2D}}$	$\frac{\mathcal{L}_N^{3D}}{\mathcal{L}_N^{2D}}$
1	528	0.59	2.15	4.02	2.88	3.11	2.61	0.77	0.91
2	576	0.75	2.85	5.26	4.13	3.73	3.31	0.71	0.80
3	671	0.57	2.63	4.07	2.89	3.12	2.59	0.77	0.89
4	1239	0.47	2.14	3.76	2.45	2.94	2.30	0.78	0.94
5	2148	0.75	3.50	7.37	5.74	4.53	3.96	0.61	0.69
6	1024	0.40	1.96	3.28	2.02	2.71	2.03	0.83	1.01
7	1024	0.50	2.21	3.79	2.60	3.00	2.39	0.79	0.92
8	1024	0.60	2.58	4.61	3.32	3.36	2.81	0.73	0.85

An experimental verification in three dimensions still requires a lot of research to find a good algorithm for three-dimensional placement and routing. However, the comparison with experiments in two dimensions (column $\mathcal{L}_{exp}^{2D}$ in Table 1), does show that estimates based on the non-uniform occupancy distribution are a lot more accurate than the ones based on the uniform occupancy distribution (Donath's technique). Since the extension to three dimensions does not change the estimation method fundamentally, the same result is to be expected for three-dimensional systems.

The last two columns of Table 1 show the improvement for a three-dimensional placement over a two-dimensional one for both techniques. One can see that the average interconnection length is lower for designs placed in a three-dimensional system than it is for designs placed in a two-dimensional system, especially for highly complex designs. This indicates that three-dimensional systems are beneficial for the placement of complex designs ($r > 0.5$). More detailed research on this topic can be found in [3], [18]. For designs with a low Rent exponent, there is not so much difference between two- and three-dimensional placement. In fact, designs with $r < 0.5$ can be placed in a two-dimensional system without too much difficulties.[†] A placement in three dimensions only results in a two-dimensional placement, folded up into three dimensions. Comparing the last two columns of table 1, we see that the technique based on a non-uniform occupancy distribution indeed gives comparable results for designs with $r \leqq 0.5$ while the other technique still shows a significant improvement for three-dimensional placement over two-dimensional placement. This indicates that the latter technique overestimates the average interconnection length while the results obtained by using the technique based on the non-uniform occupancy distribution clearly confirm the fact that an improvement

[†]For $r < 0.5$, the scaling factor $H(K,r)$ (Eq. 18) is smaller than the scaling factor of the size of the square grid.

can only be expected for highly complex designs.

6. Conclusion

In this paper, we have extended Donath's technique to three-dimensional systems. We have also introduced the global interconnection length distribution into the local distributions at each hierarchical level by using it as a non-uniform occupancy distribution. This way, we have obtained a very accurate average interconnection length estimation. Our results not only cover the scaling behaviour due to Rent's rule, but they also include the inherent behaviour of an optimal placement process in each hierarchical level.

The results show that it is beneficial to use three-dimensional systems for the implementation of highly complex designs and the methods described in this paper provide a way to accurately estimate interconnection lengths in such systems before they actually have to be built.

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