Estimating Logic Cell to I/O Pad Lengths in Computer Systems

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Abstract— Increasing system complexity imposes high demands on computer aided design (CAD) tools for system synthesis. Especially the layout (placement and routing) of a design has become a problem hard to solve. To find a 'good' layout, CAD tools need accurate estimators to predict area requirements, interconnection lengths, power dissipation, etc.

In this paper we address the estimation of interconnection lengths. Previous work on this subject is primarily based on a technique introduced by Donath [1] which has been improved by Stroobandt et al [2]. However, this technique only estimates interconnection lengths between two cells within the system or chip. Of equal importance to the CAD tools is the length estimation of interconnections between cells and I/O pads. This paper provides a technique to accurately estimate cell to I/O pad lengths.

I. Introduction

The production of VLSI and ULSI computer chips requires the layout (placement and routing) of the chip design on a carrier. With the advent of high level description languages such as VHDL, with the extensive use of component libraries, and with the standardization of production parameters, more and more steps in the design cycle are being automated. In the early days of chip design, manually designing a chip was still feasible. Nowadays, computer aided design (CAD) tools are indispensable to cope with the complexity and the limited time resources.

For the high demands put on system performances these days, CAD tools often lack enough flexibility. The helping hand of expert system designers is still needed for making important design decisions. Especially for the placement and routing phases extremely high demands are set. For the placement and routing to be good enough, accurate predictions of system performances are badly needed to limit the search in the vast solution space. CAD tools therefore use estimator tools [3] based on partitioning methodologies [4]. One of the most interesting parameters to estimate is the interconnection length within the placed design since it has a direct impact on area occupancy, on timing issues and clock frequency, on power dissipation, etc. This paper addresses the estimation of interconnection lengths within designs before the design is actually placed. These estimates can then be used to obtain better layouts.

Interconnection length estimates can also be useful for gaining a more fundamental insight in the placement of designs on different carriers. A lot of research performed by Van Marck and Stroobandt is aimed at evaluating three-dimensional architectures where optical channels are used for the third dimension interconnections [5, 6, 7, 8]. The possibilities of such architectures can be explored without actually having to produce the systems.

There have been many attempts to predict interconnection lengths. A first upper bound has been found by Sutherland and Oestreicher [9]. Since it is based on a random placement, it yields excessively large estimates. Donath [1] found that a hierarchical placement technique gives much better interconnection length estimates and his results have been used by several other researchers [7, 8, 10]. Donath's estimates follow the trend of experimentally obtained values but they still overestimate interconnection lengths by a factor of 2 or larger. Stroobandt et al [2] improved this technique by taking into account the inherent behaviour of a 'good' placement algorithm. Their estimates proved to be a lot more accurate.

None of the estimation techniques mentioned above includes length estimations for interconnections connecting a gate to the outside of the chip (the *external interconnections*). In section III, we will show that the estimation of external interconnection lengths is important. In section IV, we will present a way to account for these external interconnections. The obtained theoretical estimates will then be evaluated by comparing them to experimentally measured interconnection length values. But first, the key issues of Donath's technique and the extensions presented by Stroobandt et al will be highlighted.

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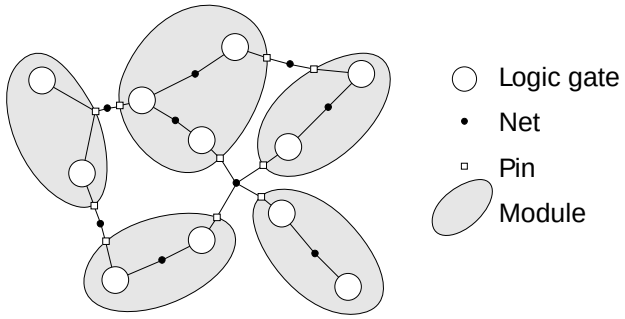

Fig. 1. Model of a partitioned design.

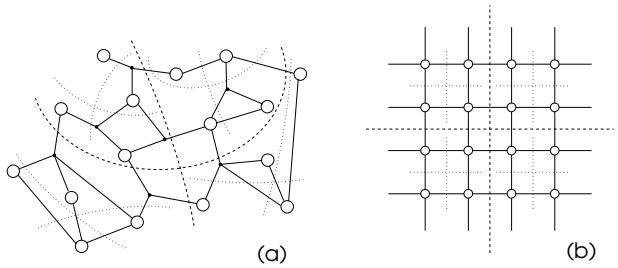

Fig. 2. Recursive partitioning scheme of the design (a) and the physical architecture (b).

II. Interconnection Length Estimations

The technique of estimating the external interconnection lengths will be presented in section IV. Since this technique is largely based on the results of previous research on internal length estimates (presented in [1] and [2]), we will first introduce the basics of the internal interconnection length estimation technique.

A. Donath's Estimation Technique

Donath estimates the average interconnection length using three models [1]: one for the design itself, one for the architecture the design will be placed in and a third model for the placement process.

A design can be represented by a set of interconnected logic gates (Fig. 1). An interconnection between gates is called a *net*. A net that is connected to more than two logic gates is called a *multi-point net*. A design can thus be represented by a bipartite graph $G_d\langle V, E\rangle$ (with $V = V_b \cup V_n$) where the vertices in one partition (V_b) represent the logic gates of the design and the vertices in the other partition (V_n) represent the nets. Such a graph can be partitioned into disjunct *modules*, each containing a subset of the gates (Fig. 1). Nets can be shared between modules. Each net (vertex in V_n) that is shared by multiple modules will be called an *external net* to those modules. An edge that crosses a module boundary connects an external net to a *pin* of the module.

The design is characterized by its interconnection complexity which can be modelled using a relationship between the number of logic gates B in a module of a partitioned design, and the number of the module's external connections (pins) P, known as Rent's rule [11, 12]:

$$P = FB^r, \tag{1}$$

where F is the average number of terminals per gate and r is called the *Rent exponent*. This exponent is a measure of the interconnection complexity of the design. Its value is bounded by 0 and 1, with increasing values for increasing interconnection complexity. Generally, r ranges from 0.47 for regular designs (such as RAM), up to 0.75 for complex designs (such as fast full custom VLSI designs) [13]. Rent's rule holds for a wide range of designs because designers tend to build their designs hierarchically, imposing the same complexity on the design at each level of hierarchy.

The architecture is modelled as a square Manhattan grid (Fig. 2(b)). In this grid, each grid point (or *cell*) corresponds to a location where one logic gate of the design can be placed. The grid lines correspond to the *channels* in which the connections between the gates can be routed. All lengths are measured using a Manhattan metric.

Donath's theoretical partitioning and placement process is based on a hierarchical placement of the design into the physical architecture. We define an *optimal placement* as one that minimizes the total interconnection length. This optimal placement should be correctly modelled by the hierarchical placement method.

At this point, it is important to note the difference between a *design* and its *implementation*. A *design* is merely a collection of interconnected logic gates. Some properties, like interconnection length, have no meaning then. The *implementation* of a design into the physical architecture, however, is the result of the placement and routing of the design in the target architecture. The logic gates of the design are implemented as *cells* in the architecture, the connections between gates routed through *channels*, and the pins mapped to the *I/O pads*. It is only after placement and routing that the aforementioned properties get their meaning.

In Donath's method, the design and the architecture are partitioned hierarchically into sub-designs and sub-architectures. Due to the symmetry of the architecture, each step in the partitioning hierarchy divides the design and the architecture into four sub-parts. Each sub-design (sub-architecture) at a hierarchical level consists itself of four sub-designs (sub-architectures) of equal size at the next (lower) level of hierarchy (Fig. 2). Each sub-design is paired recursively with a sub-architecture until all logic gates are paired with (and essentially assigned to) exactly one grid location.

The partitioning of the design into four sub-designs of equal size should be done in such a way that the partition satisfies Rent's rule. That is, we want to keep the number of interconnections between the sub-designs as low as possible. This ensures that the placement scheme is a good model for the optimal placement of the design. It is indeed obvious that, in an optimal placement, densely interconnected logic gates are placed as close as possible, resulting in clusters of such gates. Among clusters, there are fewer interconnections. This behaviour is modelled accurately by Rent's rule.

The average interconnection length is calculated separately for each hierarchical level. For this calculation, Donath assumes that the interconnection starting points are uniformly distributed over the cells of one hierarchical level. The average length at each level is then scaled with the number of connections at that level (calculated from Rent's rule) and it is this scaling which determines the final trend of the average interconnection length.

B. More Accurate Length Estimations

In [2], Stroobandt et al found that internal interconnection length estimations could be improved by introducing advance knowledge on optimal placement processes into Donath's estimation technique. This resulted in a significant improvement of the internal interconnection length estimations. Before we elaborate on this technique, we need to present some definitions.

In the remaining of this paper, we define an *interconnection length distribution* as a collection of values, indicating, for each length l, how many interconnections have length l. The sum of these values over all lengths l equals the total number of interconnections. A *normalized interconnection length distribution* denotes, for each length l, the fraction of interconnections that has length l.

By assuming that all cells are connected to all other cells, one obtains an interconnection length distribution depending only on the physical architecture the design will be placed in. We will call this the *structural distribution*. We can also assign to each length the probability that the interconnection corresponding to that length would be laid out in a real placement procedure and with a real design with the specified Rent exponent. This leads to an *occupancy distribution*. Each interconnection length distribution can be factorized as the product of the structural distribution and the occupancy distribution. Donath's assumption of a uniform distribution of interconnection starting points leads to a uniform occupancy distribution at each hierarchical level (Fig. 3(a)). The interconnection length is then only depending on the structural distribution at that level. Further on, we will show that this, in fact, is the main reason for the overestimation of interconnection lengths in Donath's technique.

By introducing a non-uniform occupancy distribution, Stroobandt et al [2] followed the intuitive notion that an optimal placement process would place interconnected gates at cells as close to each other as possible. This means that gates that are interconnected to a gate of another square at the same hierarchical level would be placed preferably near the border of the two squares. The non-uniform occupancy distribution presented by Stroobandt et al reflects this behaviour (Fig. 3(b)). The distribution also takes the design complexity into account. This is necessary since it is more difficult, even for an optimal placement process, to place complex designs than it is to place simple designs.

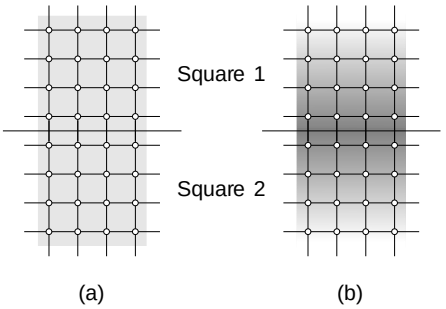

Fig. 3. Uniform occupancy distribution (a) versus non-uniform occupancy distribution (b). Darker zones have a higher probability to hold a connection at that level.

In [2], Stroobandt et al showed that the overall interconnection length distribution for a design placed in a two-dimensional square grid should be of the form

$$f(l) \sim l^{2r-3}. \tag{2}$$

This distribution shows that shorter interconnections will outnumber longer ones but the ratio largely depends on the Rent exponent. This behaviour is found using Donath's partitioning technique and is the result of the decreasing number of interconnections at higher hierarchical levels due to Rent's rule. The trend of the distribution corresponds to our notion that designs of higher complexity will lead to a higher average interconnection length since placement and routing of the design is more difficult.

Since equation 2 mainly depends on Rent's rule and thus on the complexity of the design alone, the structure of the square grid can only have a minor impact on the distribution found in equation 2 (especially for very large designs). Therefore, this distribution can be seen as the occupancy distribution of the whole design. The scalability of designs that obey Rent's rule indicates that the occupancy distribution should not depend on the size of the design, nor on the part of the design that we are looking at. On average, the length distribution of interconnections starting from any cell should follow equation 2. Equation 2 has therefore been used as the occupancy distribution at each hierarchical level and this resulted in much more accurate estimates. More details can be found in [2].

III. External Interconnection Length Estimate

The interconnection length estimation technique presented in the previous section does not include the external interconnections. These connect a cell in the interior with an I/O pad at the border of the architecture. In this section, we will show that the estimation of external interconnection lengths is equally important.

In order to obtain 'good' layouts (i.e. layouts that are close to optimal), accurate estimators are required. Most estimators use area requirements or interconnection lengths as a measure for the goodness of layouts. This leads to a weighted hypergraph $G_d\langle V, E\rangle$ with vertices in V and edges in E weighted to reflect module area requirements and/or interconnection lengths. The information in the graph can then be used in the layout process. This paper is focused on finding the weights for the edges E, especially for the external interconnections (between logic gates and pins).

For the estimation of the interconnection lengths we cannot rely on layout information (i.e. the result of measurements performed after layout) since the estimations are a means to obtain the layout. We must therefore confine ourselves to partitioning information.

For internal nets (nets that are not connected to I/O pads) the estimation technique presented in section II provides a solid estimation basis. For gate to pin interconnections (external interconnections), it is clear that the interconnection length will depend on the place of both the cell corresponding to the logic gate and the I/O pad corresponding to the pin. The technique presented in section II disregards these external interconnections. For finding the 'good' layout, however, external interconnection length estimates are quite important. Assume, for instance, that the layout tool wants to place a cluster of gates connected to a pin through a multi-point net. If we disregard the net branch to the pin, it is perfectly possible that the best place for this cluster would be in the centre of the chip (Fig. 4). In the routing phase, this will result in long interconnections to the I/O pad (generally much longer than the average internal lengths) and this can have serious implications on the chip speed, dissipation or other features. An accurate estimation of cell to I/O pad interconnection lengths could prevent the layout tool of accepting such a placement.

Another reason for introducing external interconnection length estimates is to be found in the layout process for the placement of the I/O pads. Highly complex designs need a lot of pins, resulting in the fact that most designs are pin-limited. A lot of effort is devoted to reduce the number of output pins, for instance by serializing output lines. However, pin counts still require the pin density at the chip border to be maximal, making the pin layout problem very hard. In terms of interconnection length, it may not be the best solution to place the pin of a certain net at the closest border position since this might impose longer lengths for other external interconnections. An accurate length estimate could also alleviate this pin layout problem. Since pin density should be equal at all I/O pad positions along the border of the chip, this imposes an extra restriction on the layout process and on the length estimation. In this paper, this restriction of a uniform pin density will be included in the external length calculations of section IV.

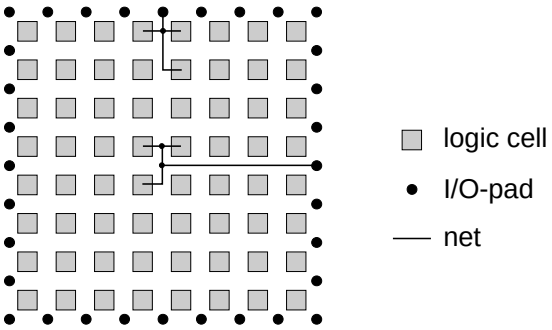

Fig. 4. The difference between a placement that takes external net branches into account and one that does not.

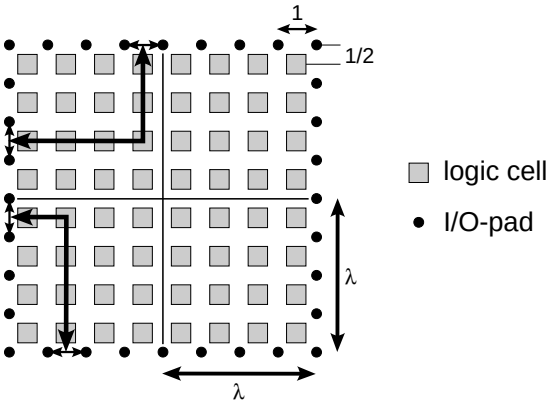

Fig. 5. Estimated length of cell to I/O pad interconnections.

IV. Average External Interconnection Length

A. Basic Assumptions

The length of an interconnection between a gate and a pin should be computed as the length between the cell where the gate is placed and the closest available I/O pad location with respect to the uniform pin density restriction. If the external interconnections were not considered during the layout phase, there is no preferred starting point for external interconnections. Then each cell has, on average, an equal amount of external interconnections starting from that cell. We can thus assume a uniform occupancy distribution. With this assumption, the pin density restriction is met if we assume I/O pad locations as in Fig. 5. In this figure, the structural external interconnection length distribution is found by assuming that an external interconnection that starts at a certain cell

leads to the closest I/O pad location(s) of either the closest border side or the second closest border side, with equal probability. One can easily verify that

1. the uniform pin density restriction is met;
2. the resulting average length remains as short as possible under the assumption of uniformly distributed interconnection starting points.

The average external interconnection length for square grids with side 2λ can then be found to be

$$\mathcal{L}_{ext} = \frac{\sum_{i=0}^{\lambda-1}\sum_{j=0}^{\lambda-1}\left(\frac{1}{2}(i+1)+\frac{1}{2}(j+1)\right)}{\lambda^2} \quad (3)$$

$$= \frac{\sum_{i=0}^{\lambda-1}(i+1)}{\lambda} \quad (4)$$

$$= \frac{\lambda+1}{2.} \quad (5)$$

B. Including Optimal Placement Information

The average external interconnection length found in the previous subsection obviously is too large if the placement program takes external interconnections into account. For large designs, external interconnections will be mainly routed in a ring close to the border of the chip and the average length will not increase linearly with the design size. Therefore, external interconnection lengths will be much shorter than equation 5 predicts. Moreover, the external interconnection length estimates should depend on the interconnection complexity and thus on the Rent exponent. For complex designs, finding a good layout will be more difficult than for simple designs, resulting in a different interconnection length behaviour for both designs. This observation is very similar to the observation made by Stroobandt et al [2] regarding the internal interconnections (see section II.B). As in section II.B, we will therefore introduce a non-uniform occupancy distribution in order to obey the intuitive notion that cells close to the border should hold more external interconnections than cells in the centre of the architecture. Since we stated in section II.B that every cell in the architecture should have the same occupancy distribution, this statement should also hold for the external interconnections. For this reason, we believe the occupancy distribution for external interconnections should be equal to the one presented in equation 2. Therefore we should multiply each term in equation 4 by the occupancy distribution (equation 2, with $l = i+1$) and normalize accordingly to obtain

$$\mathcal{L}_{ext} = \frac{\sum_{i=0}^{\lambda-1}(i+1)^{2r-2}}{\sum_{i=0}^{\lambda-1}(i+1)^{2r-3}}. \quad (6)$$

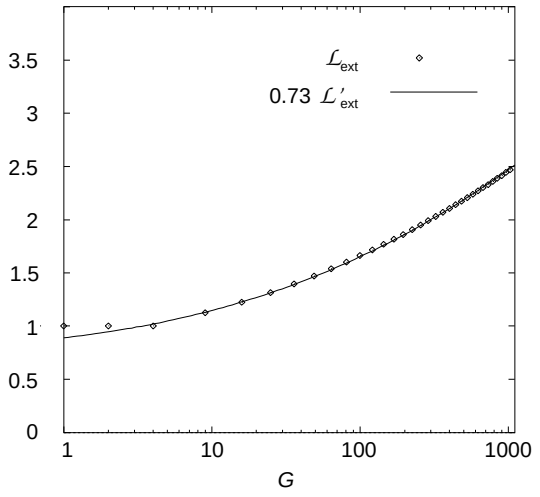

Fig. 6. Evaluation of the approximation of the average external interconnection length in function of the total number of gates G of a design ($r = 0.6$).

The sums in equation 6 can not be computed analytically as a function of λ. Yet, if we want to compare our results with those of the previous section (equation 5), both numerically and theoretically, an analytical form of the average interconnection length is needed. A way around this problem is to approximate equation 6 by

$$\mathcal{L}'_{ext} = \frac{\int_{i=0}^{\lambda}(i+1)^{2r-2}di}{\int_{i=0}^{\lambda}(i+1)^{2r-3}di}$$

$$= \frac{2\,(r-1)\left((\lambda+1)^{2\,r-1}-1\right)}{(2\,r-1)\left((\lambda+1)^{2\,r-2}-1\right)}. \quad (7)$$

In order to evaluate the error made by this approximation, we calculated the external distribution numerically using equation 6 for designs with different numbers of gates and a Rent exponent r equal to 0.60. The results can be seen in Fig. 6. This figure shows that, with the introduction of a scaling factor equal to 0.73[1], the approximated estimation (equation 7) coincides with the theoretical data (equation 6) for a wide range of the number of gates ($4 \leq G \leq 1024$). A good approximation for the external interconnection length estimation represented by equation 6 should therefore be given by

$$\mathcal{L}_{ext} = 0.73\,\mathcal{L}'_{ext} = \frac{1.46\,(r-1)\left((\lambda+1)^{2\,r-1}-1\right)}{(2\,r-1)\left((\lambda+1)^{2\,r-2}-1\right)}. \quad (8)$$

The main difference between equations 5 and 8 is to be found in the asymptotic behaviour for $\lambda \to \infty$. Equation 5

[1] A more thorough examination shows that the scaling factor slightly depends on the Rent exponent r and equals $0.25\,r^2 - 0.15\,r + 0.73$ for normal values of r ($0.4 \leq r \leq 0.8$).

scales with λ. Equation 8 behaves differently for $r < 0.5$ and $r > 0.5$. For $r < 0.5$, it produces a constant average length for large designs. This corresponds to the notion that designs with a Rent exponent lower than 0.5 are basically two-dimensional [2]. The number of external interconnections (pins) increases slower than the chip size which results in the fact that all external interconnections can be placed near the border of the chip. Increasing the chip size then does not affect the interconnection length. For $r > 0.5$, equation 8 scales with λ^{2r-1}. In this case, interconnection lengths still increase with the chip size but slower than linearly. As could be expected, this scaling behaviour is identical to the scaling behaviour found for internal interconnections [2].

V. Experimental Verification and Results

In the previous section we found equation 8 as a length estimation for external interconnections. This equation was obtained by extending the techniques described in [2] to include external interconnections.

In order to validate our new external interconnection length estimations, we set up some experiments using the ISCAS85 and ISCAS89 benchmark circuits. For each of the benchmark circuits, the total number of gates G, the number of external pins P, and the estimated Rent exponent r (obtained by using 'ratiocut' [4, 14]) are presented in table I.

The benchmark designs were placed in a Manhattan grid using *Simulated Annealing* [15]. Our simulated annealing program searches for the placement resulting in the lowest total interconnection length. The resulting experimental placements are therefore good samples of the optimal placement. The uniform pin density requirement is taken into account by the cost function.

During the placement by the simulated annealing program, the interconnection lengths are measured for the internal and external interconnections separately. The length of multi-point nets is calculated by taking into account the Steiner tree length. The external part of multi-point nets connected to a pin is calculated as the difference between the Steiner length of the net with and without the connection to the pin. The experimentally measured external interconnection lengths are presented in table I (column $\mathcal{L}_E$). This table also shows the theoretical estimates of the average external interconnection length. $\mathcal{L}_N$ is the theoretical external interconnection length estimate if the external lengths would be discarded by the (optimal) placement program (equation 5); $\mathcal{L}_T$ is our theoretical external interconnection length estimate (equation 8). It is clear from the results shown that both the experimentally obtained values and our estimates are considerably smaller than the values found for $\mathcal{L}_N$. This clearly shows the importance of including external interconnections into the CAD estimator tools.

TABLE I
Experimental results. Circuits whose name begins with a 'c' are ISCAS85 combinatorial benchmarks, the others are ISCAS89 sequential benchmarks. The benchmarks with extension 'out' have been technology mapped using SIS before placement.

Name	G	P	r	$\mathcal{L}_E$	$\mathcal{L}_N$	$\mathcal{L}_T$
c432	160	43	0.62	2.00	3.66	1.82
c499	202	73	0.55	1.30	4.05	1.79
c880	383	86	0.57	2.05	5.39	2.02
c1355	546	73	0.50	1.51	6.34	1.98
c1908	880	58	0.52	2.41	7.92	2.17
c432nr	157	43	0.62	1.86	3.63	1.82
c499nr	202	73	0.60	1.29	4.05	1.87
c1355nr	546	73	0.50	1.58	6.34	1.98
c1908nr	878	58	0.51	2.36	7.91	2.14
s208.1	112	11	0.39	1.73	3.15	1.46
s298	133	9	0.42	1.00	3.38	1.52
s344	175	20	0.34	1.72	3.81	1.50
s349	176	20	0.38	1.72	3.82	1.54
s382	179	9	0.34	1.00	3.84	1.50
s386	165	14	0.57	1.86	3.71	1.76
s420.1	234	19	0.38	1.84	4.32	1.59
s444	202	9	0.35	1.11	4.05	1.53
s510	217	26	0.66	1.84	4.18	2.00
s526	214	9	0.48	1.00	4.16	1.70
s526n	215	9	0.49	1.00	4.17	1.71
s641	398	59	0.52	1.20	5.49	1.93
s713	412	58	0.46	1.17	5.57	1.83
s820	294	37	0.57	2.03	4.79	1.94
s832	292	37	0.58	2.25	4.77	1.95
s838.1	478	35	0.38	2.54	5.97	1.72
s953	424	39	0.68	1.85	5.65	2.34
s1196	547	28	0.64	3.18	6.35	2.34
s1238	526	28	0.63	2.15	6.23	2.29
s1423	731	22	0.38	2.18	7.26	1.80
s1488	659	27	0.62	2.11	6.92	2.36
s1494	653	27	0.61	1.89	6.89	2.33
s208.1.out	41	11	0.48	1.09	2.10	1.34
s298.out	71	9	0.36	1.00	2.61	1.36
s344.out	88	20	0.44	1.65	2.85	1.46
s349.out	84	20	0.47	1.75	2.79	1.48
s382.out	94	9	0.37	1.22	2.92	1.42
s420.1.out	93	19	0.49	1.26	2.91	1.52
s838.1.out	199	35	0.52	1.71	4.03	1.74
s1196.out	327	28	0.54	2.25	5.02	1.91
s1238.out	339	28	0.54	2.00	5.10	1.92
s1423.out	347	22	0.47	2.05	5.16	1.80
s1488.out	353	27	0.45	2.96	5.20	1.77
s1494.out	358	27	0.45	3.08	5.23	1.78

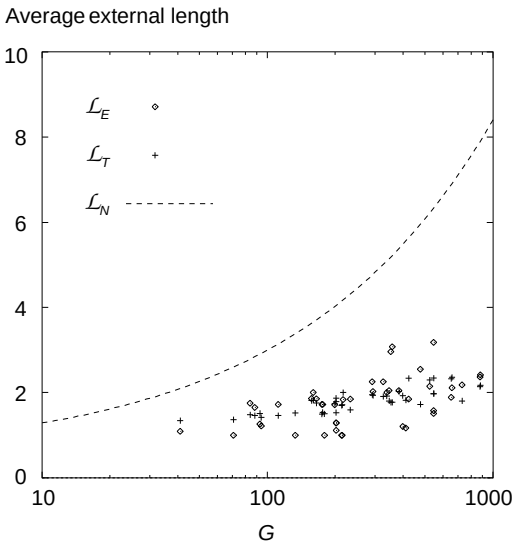

Fig. 7. Experimental validation ($\mathcal{L}_E$) of the theoretical external interconnection length estimates ($\mathcal{L}_T$). The different trend in $\mathcal{L}_N$ (external length when external interconnections are discarded during placement) shows that including external interconnection lengths into the estimations is important.

Table I also shows that the obtained theoretical estimates $\mathcal{L}_T$ are closely related to the experimentally obtained values. The accuracy of the results can be appreciated from Fig. 7. In this figure, $\mathcal{L}_T$ and $\mathcal{L}_E$ are shown as a function of the number of gates G of the benchmark designs. It can be clearly seen that they follow the same trend and are closely related to each other for most benchmarks. This gives us confidence to say that the introduction of the occupancy distribution as described in section IV.B really captures the behaviour of a 'good' placement program where interconnection lengths are concerned. It can also be seen from the figure that $\mathcal{L}_N$ follows a totally different trend. This shows that, especially for large designs, including external interconnections into the estimations is important.

VI. Conclusions

By introducing a suitable occupancy distribution for the interconnection lengths in a placed design, we found accurate estimates of the interconnection lengths of cell to I/O pad interconnections. Such estimates are important for the use in estimator tools to help the CAD tools for placement and routing of digital designs finding a better layout. This in turn results in improved overall performance of the produced system.

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