Interconnection length distributions in 3-dimensional anisotropic systems

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Abstract

In recent years we have witnessed the arrival of the technology necessary for building 3-dimensional electronic systems [1]. These systems could consist of a number of 2-dimensional electronic boards, stacked on top of each other. A large number of vertical interconnections, distributed over the surface of the boards, interconnect adjacent electronic planes. The primary alleged advantage of such systems over conventional 2-dimensional ones is the reduction of signal latency due to reduced interconnection lengths. This paper is concerned with modeling 3-dimensional electronic systems, and estimating layout properties like interconnection length distributions.

Keywords: Interconnection length, Rent's rule, 3-dimensional anisotropic systems

1 Introduction

The availability of the technology, allowing high-density interconnections in three dimensions, opens the perspective to realize systems that are demonstrably better than current-day electronic systems. In particular, the ability to realize massive interconnections between parallel electronic planes opens the way to create layouts of designs, having much more complex interconnection topologies. It also results in a reduction of the interconnection lengths compared to traditional 2-dimensional topologies, thus leading to faster, and more compact systems. Our research activities are focused on the modeling of 3-dimensional architectures, and the extraction of relevant layout properties like interconnection lengths and area (space) requirements.

Current-day 3-dimensional systems have different interconnection properties in the three dimensions. These systems are therefore said to be *anisotropic*. Since this will likely be the case for future systems as well, our model for the 3-dimensional architectures takes into account these different interconnection properties.

A framework has been developed [2] which allows an estimation of the average interconnection lengths in systems with varying interconnection densities. However, properties like routing area requirements depend on interconnection lengths in a non-linear way. In those cases, knowledge of the average interconnection length is not enough. In this paper we use interconnection length distributions in 3-dimensional anisotropic systems as an evaluation measure.

The models for the electronic design, the 3-dimensional physical architecture in which the design is to be implemented, and the layout process are described in section 2. In section 3 we describe the mathematical techniques used to derive an accurate estimation of the interconnection length distribution associated with such systems. An example of the application of the proposed techniques and the resulting interconnection length distributions follow in section 4. There, a brief discussion is given on the different parameters and their influence on the interconnection length.

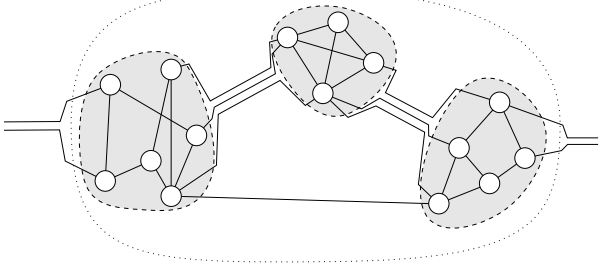

Figure 1: Hierarchical model of a design.

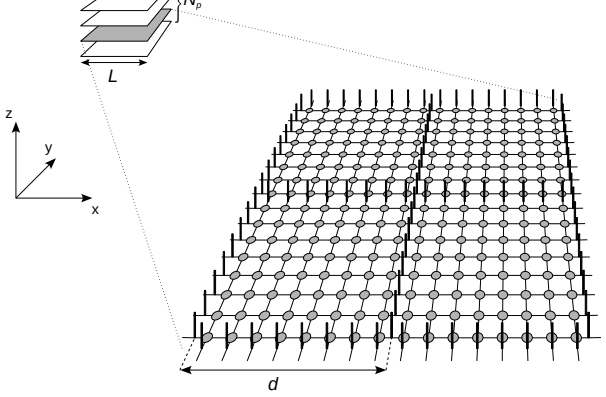

Figure 2: Model of the physical architecture of a 3-dimensional system.

2 Mathematical models

Basically, there are three major aspects involved when designing a system. The first aspect, the *logic design*, consists of a number of interconnected logic gates. The second aspect is a description of the physical space, called the *physical architecture*, in which the logic gates and the interconnections between them are implemented electronically. The transformation of the design into the physical architecture is called the *layout process*. To assess the layout properties of a system we need to model the design, the physical architecture and the layout process. These models are an extension of the work of Donath in two dimensions [3] towards 3-dimensional anisotropic systems.

Since we want to evaluate 3-dimensional architectures for a wide variety of designs, the model for the designs should not be too restricted. However, we want to have a clear view on the complexity of the interconnection topology of the design. It is intuitively clear that an increased interconnection complexity will result in longer interconnections in the realized system. The design is characterized by an empirically derived law, known as *Rent's rule* [4, 5, 6]. The associated *Rent exponent* r is a measure for the interconnection complexity of the design. The value of r varies from 0.4 for simple regular designs (such as Random Access Memories), up to 0.8 for complex designs (such as fast full custom VLSI designs). Rent's rule is based on a partitioning of the design and on the hierarchical "self-similarity" of designs (figure 1). A design can thus be modeled hierarchically as an interconnection of subdesigns [3, 7]. At the lowest hierarchical level each subdesign consists of a single logic gate.

The physical architecture is modeled as a collection of *grid points*, with *channels* between them. The grid points correspond to positions in the physical space, where logic gates are placed, and the channels correspond to areas in the physical space, where the interconnections between logic gates are laid out. The model for the physical architecture is a 3-dimensional grid: a stack of 2-dimensional grids, with a limited number of vertical channels between adjacent planes [2]. These channels are distributed over the planes, forming a coarser grid with spacing d (figure 2). The model thus includes the inherent anisotropy.

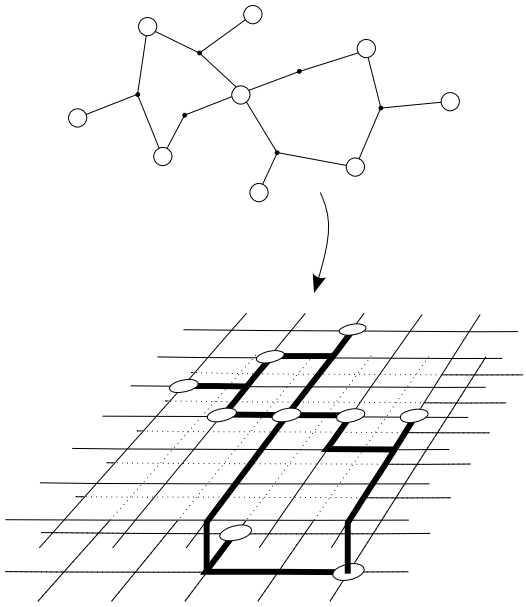

Figure 3: The embedding of a design into a physical architecture.

In many ways, the layout process is the most difficult aspect to model, since it can only rely on the limited information contained in the models for the design and the physical architecture. The layout process is modeled as an *embedding* of the design in the physical architecture, represented by figure 3. This process consists of recursively partitioning the design and the physical architecture into subdesigns and subarchitectures, and then assigning each subdesign to a subarchitecture [3, 8]. The final recursion step then assigns a single logic gate to a single position in the physical architecture. During this process, also the interconnections between the logic gates are laid out, minimizing their lengths. So the layout process includes both placement and routing.

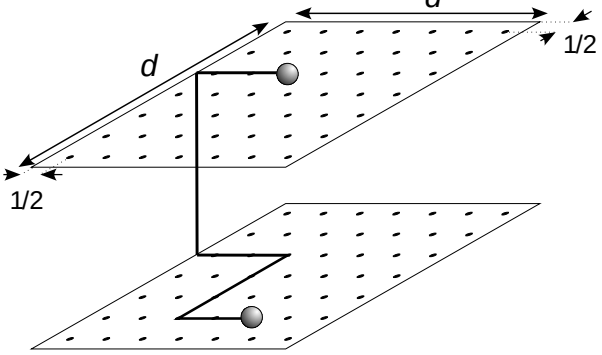

Figure 4: An interconnection that has to make a detour in the anisotropic grid.

3 Interconnection length distribution

We want to estimate the interconnection length distribution associated with the embedding performed by the layout process. If we do this for several designs and several physical architectures, we can compare the results. This way, we will be able to assess the properties of 3-dimensional architectures and to see the influence of the parameters of the design and the physical architecture.

The calculation of the interconnection length distribution for an anisotropic grid is an extension of the method of Donath [7, 5] towards 3-dimensional anisotropic systems. On each recursive level of the model for the layout process, the number of possible interconnections with length k is counted. However, we must take into account that points that are connected via vertical links in the 3-dimensional anisotropic grid are typically further apart, since a "detour" to the edges of the squares with side d must be made (figure 4).

Consider a collection of interconnected logic gates, embedded into an anisotropic physical architecture. Each interconnection between two placed logic gates is routed through the channels of the architecture. Interconnections that use a vertical channel, typically have a longer interconnection length. The interconnection length will be expressed as a multiple of the unit length (the distance between two horizontally aligned gridpoints) by introducing a *vertical cost* C_v. This vertical cost takes into account the fact that a vertical channel is longer than a horizontal one. To keep the calculations simple, we assume C_v to be an integer.

Next, we consider the *distribution* of interconnection lengths over the entire circuit. The use of *generating polynomials* to represent this distribution enables us to use computer aided symbolic calculations. To determine the overall distribution, we use the fact that the model for the layout process is hierarchical. This allows us to partition the collection of all the interconnections of a placed and routed design, into separate classes for each hierarchical level in the layout process. Rent's rule can then be used to find the *number* of interconnections at that level. For the calculation of the actual interconnection length distribution at the hierarchical level k, we assume that for each interconnection between two subdesigns, the endpoints are independently and uniformly distributed across the grid points of the corresponding subarchitectures. For each possible combination of endpoints, we determine the corresponding interconnection length by a careful case analysis. Enumerating and combining all these interconnection lengths then results in an interconnection length distribution for that hierarchical level. Merging the distributions pertaining to the individual hierarchical levels yields the overall distribution. This distribution depends on both the parameters of the design (described by r) and those of the physical architecture (size L, vertical channel spacing d, number of planes N_p).

4 Results

With the models and the mathematical method described above, we can assess the influence of the various parameters. The most important ones are the interconnection complexity of the design (described by the Rent exponent r), the spacing d between the vertical interconnections, and the vertical cost C_v. The major result is that 3-dimensional architectures with a sufficiently small spacing d and vertical cost C_v lead to smaller interconnection lengths. Furthermore, such an architecture is especially useful (in comparison to 2-dimensional ones) if the interconnection complexity of the design is sufficiently high. More conclusions, obtained for optoelectronic architectures, can be found in [9].

We will present some results of our technique, when applied to the physical architecture presented in [1]. This is a 3-dimensional all-electronic architecture. We can model this architecture as an anisotropic grid (with size $L = 1896$ unit lengths, distance $d = 316$, vertical cost $C_v = 80$, and number of horizontal planes $N_p = 40$). Our calculation technique requires that most of the parameters have a value that is a power of 2. Therefore, the closest model we can provide has $L = 2048$, $d = 256$, $C_v = 80$, and $N_p = 64$. We consider a design with 256^3 nodes and a Rent exponent $r = 0.65$. It can be implemented in the proposed architectural model if this architecture has at least 4 horizontal planes. In figure 5, we show the calculated interconnection length distributions for $N_p = 4$, 16, 64, and 256 (cubic grid). The dotted line represents the 2-dimensional case. We see that for a low number of horizontal planes, the interconnection length dis-

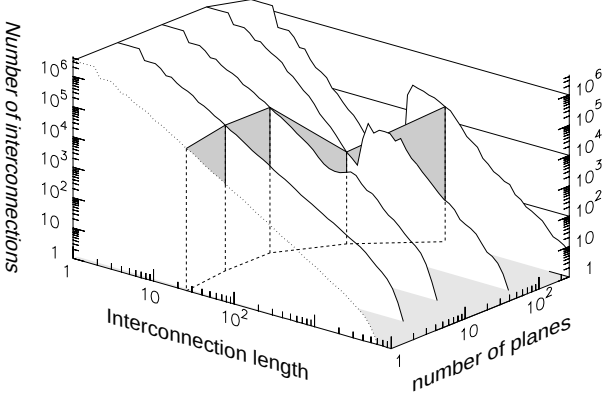

Figure 5: Interconnection length distribution and average interconnection length for the architecture presented in [1], for $r = 0.65$ and $d = 256$.

tribution is almost exponential. While increasing the number of planes, a peak emerges for high interconnection lengths. This is due to the high vertical cost. Every interconnection, forced to go through a vertical channel, has a very high interconnection length.

In figure 5, the average interconnection length is also shown (greyed vertical plane). For an increasing number of planes, the average interconnection length decreases to a minimal value and then rapidly increases. It thus is beneficial to implement the design in the 3-dimensional architecture, even with this high vertical cost. Yet, the number of horizontal planes should be kept small (the optimal value being somewhere around 16)[1].

5 Conclusion

In this paper we have described the models for 3-dimensional anisotropic systems, emphasising the applicability on 3-dimensional electronic systems. The mathematical techniques used to derive an accurate estimation of the interconnection length distribution associated with such systems, lead to an estimation of the interconnection length for the 3-dimensional anisotropic, electronic system described by [1]. Our model can also be used to search for the bottlenecks within the architecture by varying the parameters and thus can be used for an optimization of the architecture. The results show that this architecture reduces the number of long interconnections in the interconnection length distribution (and the average interconnection length) compared to a two-dimensional architecture. The benefits disappear if the number of planes becomes too large.

[1] Note that this result also depends on the Rent exponent r of the design and the spacing d of the vertical channels (a higher r and a smaller d increase the value of the optimal number of planes).

6 Acknowledgements

This research is carried out at the Department of Electronics and Information Systems at the University of Ghent, Belgium. The work of H. Van Marck is supported by an Inter University Attraction Poles research program on optical computing of the Belgian Government. D. Stroobandt is Research Assistant with the Belgian National Fund for Scientific Research.

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