Towards An Extension of Rent's Rule for Describing Local Variations in Interconnection Complexity

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Abstract

Important layout properties of electronic designs include space requirements and interconnection length values. Many techniques used to assess these properties are based on a complexity measure known as Rent's rule. However, we show that Rent's rule as it has been defined, can not account for local differences in the interconnection complexity of a design. We propose a modification of Rent's rule remedying this limitation. Our modification takes into account variations of interconnection complexity between hierarchical levels. We also can describe local complexity variations over the design, resulting in a more accurate interconnection complexity measure. Results obtained from applying this extension, by means of a computer program, are presented.

Keywords: 3-D architecture, interconnection length distribution, interconnection complexity, Rent's rule.

1 Introduction

Creating a physical layout of an electronic (or an electro-optical) design, involves placement and interconnection of elementary blocks on a carrier. Important properties of such layouts are area (or space) requirements and interconnection lengths. The ability to predict those properties, without actually having to perform the placement and routing itself, is important for the following reasons:

- Most placement algorithms use estimates for interconnection lengths and area requirements to limit the search in the solution space [SP86],[KP89].
- The predictions offer a way to gain a more fundamental insight in the placement of designs on different carriers.

Many attempts to predict area requirements [Gam81] and interconnection lengths [Don79], [Feu82], [Don81], [Fer85], [CC91] are based on a relationship between the number of elementary blocks B in a module of a partitioned design, and its number of external connections P, known as Rent's rule [LR71]. It states that

$$P = CB^r,$$

where C is the average number of interconnections per block, and r is the Rent exponent. This exponent is a measure of the interconnection complexity of the design. The Rent exponent can be obtained by a partitioning of the design. It is based on the hierarchical "self-similarity" of designs, and therefore it is closely linked with fractal geometry and a fractal dimension [Man83] [Chr1a] [CS90].

Once the Rent exponent has been obtained, the information on the interconnection complexity of the design is compressed into one number r between 0 and 1.

With this Rent exponent r predictions about an actual placement and routing on an arbitrary carrier (the physical architecture) can be made [Mar94]. These predictions allow us to choose the best physical architecture to implement the design in, without having to perform a placement procedure for every possibility. Furthermore, if we know the Rent exponent of some benchmark designs, it is possible to estimate the Rent exponent of any new design having almost the same characteristic features of the interconnection. This estimated Rent exponent results in predictions of layout properties leading to a first (fast) placement. A new Rent exponent can then be computed to predict the final layout properties.

The main problem with Rent's rule is that it does not reflect local fluctuations of the interconnection complexity in the design, and is generally not scalable. Consider for example a design consisting of two separate parts, having Rent exponents r_1 and r_2 (with $r_1 < r_2$). Rent's rule is unable to deal properly with such designs. The Rent exponent r of the combined parts will lie somewhere between r_1 and r_2. This could lead to wrong conclusions in estimating some layout properties.

We propose some ideas for a modification of Rent's rule that makes the latter scalable, and allows to account for local variations of the interconnection complexity. Our modified Rent exponent should be able to deal with both locality in the hierarchy and locality in space.

First, some formal definitions are presented for a better understanding. Next, the problem of variation in interconnection complexity over the different hierarchical levels and over different parts in the design, is discussed. An extension of the Rent exponent to deal with locality in hierarchy, is presented in section 3.1. Section 3.2 gives a discussion on locality in space and section 4 shows another way to determine

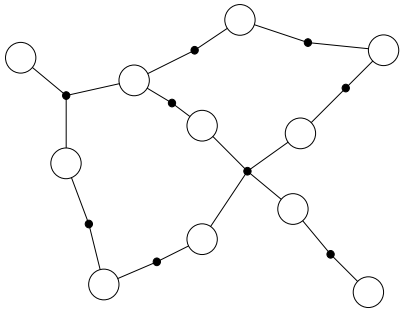

Figure 1: Model of a design consisting of blocks and nets.

the Rent exponent of a given design. We also show that this technique can easily be extended to derive a local Rent exponent, capable of dealing with variations in the interconnection complexity over different parts in the design. In section 5 some results are shown for a number of benchmark designs and a conclusion follows in section 6.

2 Definitions

Basically, our model for designs consists of a number of interconnected *elementary blocks*. In an electronic design these blocks can be transistors, logic gates, logic cells, or devices. Interconnections between blocks are called *nets*. Through these nets, information is transported from one block to another. Note that nets can transport information to multiple blocks. Such nets are called *multipoint nets* (in addition to nets that are point-to-point connections). In figure 1 the various elements of our model are shown.

A design can be described mathematically by a graph $G = \langle V, E \rangle$, where V denotes a set of vertices and E a set of edges. The graph G is bipartite ($V = V_b \cup V_n$) and is called the *design graph*. The blocks in the design are associated with the

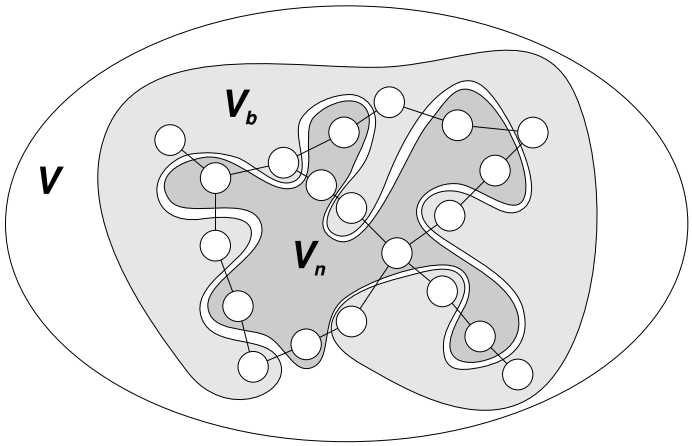

Figure 2: Design graph associated with the design model of figure 1.

vertices in V_b, and the nets with the vertices in V_n. A block b, with associated vertex $v_b \in V_b$, is connected to a net n, with associated vertex $v_n \in V_n$, if there exists an edge $e \in E$ that connects v_b and v_n. Figure 2 shows the graph associated with the design model presented in figure 1.

Modules are defined as a set of interconnected blocks. Modules are thus associated with subsets $V_m = V_{m,b} \cup V_{m,n}$ of $V = V_B \cup V_n$. The set $V_{m,b}$ contains all vertices $v_b \in V_b$ associated with the blocks in the module m. The set $V_{m,n}$ contains all vertices $v_n \in V_n$ (associated with nets) for which there exists an edge $e \in E$ that connects v_n with a vertex $v_b \in V_{m,b}$. Nets that connect blocks of different modules are present in all of these modules. Thus, the associated sets V_m and $V_{m'}$ of two modules m and m' are not necessarily disjoint. For each module m, each net associated with a vertex $v_n \in (V_m \cap V_{m'})$ will be connected to something we call *pins*. So there is one pin for each $v_n \in V_{m,n}$ that has an edge e that connects v_n to a vertex v_b of another module. These pins are the interfaces of modules (see figure 3).

With this in mind, a formal definition of Rent's rule can be given [LR71]. Con-

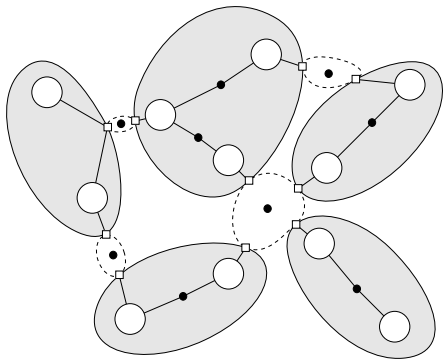

Figure 3: Partition of the design model of figure 1.

sider the partitions of the design graph in modules with the restriction that a predefined maximum number of pins per module (P_{max}) and a predefined maximum number of modules (M_{max}) are not exceeded. Consider a set of values $P_{max,1}, \ldots, P_{max,k}$. For each value $P_{max,i}$, generate a sequence of partitions with successively smaller values of M_{max}, until the last value of M_{max}, permitting a successful partition, is reached. Eventually this will result in partitions with a small number of edges crossing module boundaries, for a certain number of blocks per module. This is due to the successive lowering of M_{max}, which forces the partitioning to combine more blocks into one module without increasing the number of pins. This way, highly interconnected sets of blocks will be preferably clustered.

Using this partitioning, Rent's rule states that for general electronic designs, the following equation holds:

$$P_m = C\, B_m^r$$

with

P_m = the average number of pins per module;

B_m = the average number of blocks per module;

r = the Rent exponent;

C = the average number of interconnections per block.

The Rent exponent r is then computed by plotting the P_m versus B_m relationship in a log-log diagram for every value of P_{max}, and then fitting a line on the plotted points. The slope r of this line gives an estimation of the Rent exponent. The value of r varies from 0.4 for very simple and regular interconnections as found in a RAM-chip, up to 0.8 for complex, irregular interconnections generally attributed to "fast logic"-chips.

The main reason for the applicability of Rent's rule, is that electronic designs are built hierarchically. Modules on a hierarchical level i are constructed with sets of blocks and nets on the hierarchical level $i-1$. Each level of hierarchy exhibits more or less the same interconnection complexity. This is a consequence of building designs step by step. At each step, the complexity of the design process will be kept more or less the same. If this were not so, the designer would divide a more complex part into subparts, each of more or less equal complexity. This leads to a sort of "self-similarity" within designs (see figure 4). It also is the reason why B_m (which is a measure for the hierarchical level in the design) scales logarithmic with P_m. Note that if we define a hierarchical level i as the level where modules contain i blocks, the hierarchical levels will roughly follow the partitions for different values of P_{max}. This is true for highly self-similar designs.

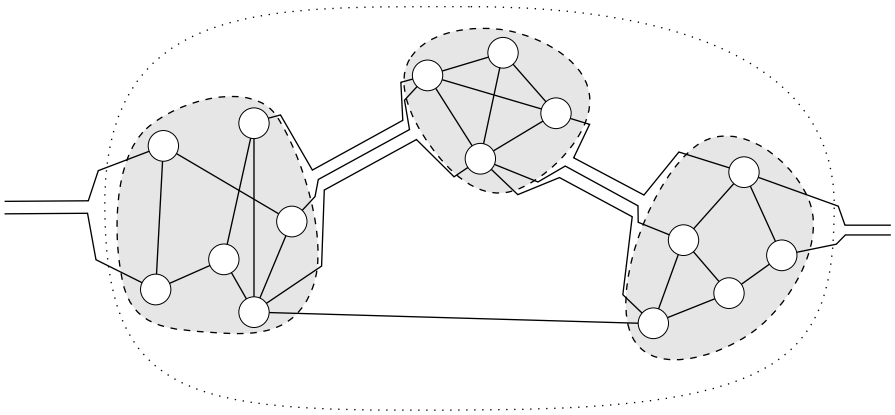

Figure 4: Hierarchy in designs.

3 Locality of interconnection complexity

If we want to make predictions of layout properties of a design, the Rent exponent could be used as a measure for the interconnection complexity. However, we must be aware that the Rent exponent does not take into account local interconnection complexity variations. Yet, on some hierarchical levels or for some blocks in the design, interconnection complexity can be quite different from the others. These variations are due to what we call *locality in hierarchy*, and *locality in space*, respectively. We will now elaborate on these issues.

3.1 Locality in hierarchy

Many current-day designs are *pin limited*. This means that the lower bound on the perimeter of the designs (which is proportional to the number of pins) imposes a mininal die area that is higher than the minimal area needed to place and route the design. So designers must keep the number of pins low. This is possible because there is a trade-off between time-complexity and area-complexity. For instance, an

eight-bit output bus can be addressed in a serial or in a parallel way. In the serial case, only one pin is needed but data transfer will take eight clock cycles, while in the parallel case, eight pins are needed and data transfer will only take one clock cycle. This trade-off between complexity in time and complexity in area is clearly present at the highest hierarchical level (where the whole design is considered as one module). The number of pins on this level, and thus the associated interconnection complexity, can differ a lot from the interconnection complexity on lower hierarchical levels. Even worse, depending on the choices the designer has taken to alleviate the pin limitations, we will have a different number of pins P on the highest hierarchical level. This leads to another Rent exponent r, while the internal interconnection complexity is roughly the same.

The main problem is that Rent's rule is not able to describe an interconnection complexity varying over the different hierarchical levels. To allow for this, we could rewrite Rent's rule as

$$P_m = C B_m^{r(B_m)},$$

with $r(B_m)$ a function of B_m. The Rent exponent would be given by the slope in the log-log diagram of P_m versus B_m:

$$r(B_m) = \frac{\partial \log(P_m)}{\partial \log(B_m)}.$$

With this definition, Rent's rule can be interpreted as a first order approximation.

3.2 Locality in space

Even if we allow the Rent exponent to vary over hierarchical levels, thus introducing a Rent exponent function, Rent's rule is only applicable to designs of a uniform

interconnection complexity. There is no way of distinguishing more complex parts of the design from simpler ones. Yet, a common processor has a highly complex ALU, but also a more regular register file. This shows that the interconnection complexity can vary a lot within one design, even within one level of hierarchy.

Suppose that we can identify two parts in a design (each in one module for the same value of P_{max}), having a different interconnection complexity. For each part, Rent's rule states [LR71]

$$P_i = C\, B_i{}^{r_i},$$

where $i = 1, 2$. In figure 5 an example is given with $P_1 = P_2 = P_{max} = 7$. Part 1 is much more complex than part 2. For this reason, module 1 contains fewer blocks than module 2 (two blocks against five). The average number of interconnections per block (C) is 4. Applying Rent's rule for both modules results in: $r_1 \approx 0.8$ (complex) and $r_2 \approx 0.35$ (not complex). In [LR71] the P_m and B_m values (corresponding to P_{max}) in the P versus B plot are computed as

$$P_m = \frac{\sum_{i=1}^{n} P_i}{n} = 7$$

and

$$B_m = \frac{\sum_{i=1}^{n} B_i}{n}.$$

If the other modules in the design contain three or four blocks (moderately complex) then $B_m \approx 3.5$. The value of r for the whole design follows from Rent's rule:

$$r = log_{3.5}(7/4) \approx 0.44.$$

Consider the placement of the design presented in figure 5 in a physical architecture. This leads to a certain interconnection length distribution f_k, i.e. the number

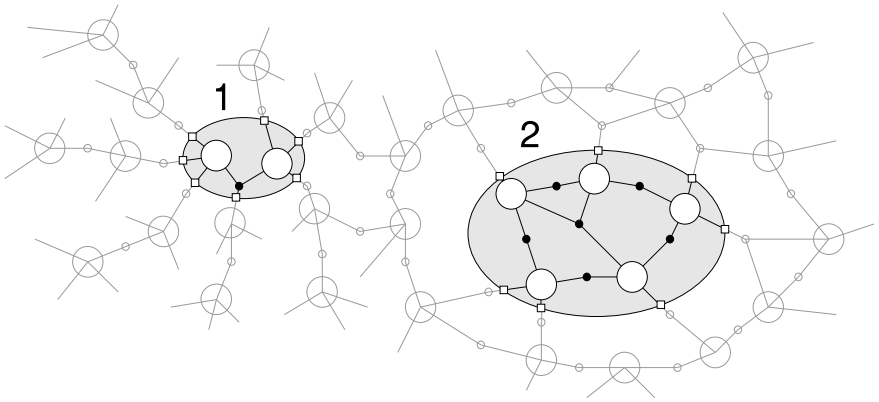

Figure 5: Example of a part of a design with a local variation in interconnection complexity.

of interconnections with a length k. The parameter of this distribution depends on the complexity of the design, for it is clear that the more complex a design is (i.e. the higher the value of r), the higher the average interconnection length will be. Consider another design with the same number of vertices and the same average number of interconnections per block C. Opposed to the design shown in figure 5 the interconnection complexity is now uniform throughout the design, with $r = 0.44$. A placement of this design in the same physical architecture leads to a distribution f'_k. Altough both designs have the same r, the interconnection length distributions f_k and f'_k will be significantly different in general. This means that the interconnection length distribution cannot be expressed as a function of r and C alone. We thus need an extension of Rent's rule to be able to describe designs of varying interconnection complexity. In order to do so, we will reveal another way to compute Rent's exponent in section 4, and we will show that we can define a local Rent exponent this way.

4 Local Rent exponent

Using Rent's rule, we can show [Don81] that the distribution f_k of interconnection lengths for a "good" two-dimensional placement on a square Manhattan grid is of the form $f_k \approx c\,k^{2r-3}$ $(1 \leq k \leq L)$, and $f_k \approx 0$ $(k > L)$ [Don79]. Here, L is a kind of cross-section of the physical architecture the design wille be placed in. We define a good placement as one that minimizes the total interconnection length. Furthermore, we can show [Mar95] that for a good placement in a D-dimensional Manhattan grid, the interconnection length distribution is of the form $f_k \approx c\,k^{Dr-(D+1)}$ $(1 \leq k \leq L^{2/D})$, and $f_k \approx 0$ $(k > L^{2/D})$.

This observation leads us to the following idea. The interconnection complexity of a design could be measured using the interconnection length distribution of a good placement in a Manhattan grid. The Rent exponent can then be obtained from the slope of the line fitted to f_k in a log-log plot. If we consider f_k of the entire design, then this is compatible with the Rent exponent defined in [LR71].

The benefit of our method for obtaining Rent's exponent lies in the ability to define a *local Rent exponent* in an easy way. Consider a vertex v_b from the graph defined in section 2. For each length l, count the number of interconnections N_l of length l that part from vertex v_b. Plot N_l versus l in a log-log diagram and find the best-fitting line on the plotted points. We define the local Rent exponent around the vertex v_b by stating that $D\,r_l - (D+1)$ equals the slope of our plotted line. Equivalently, we can define a Rent exponent local to a set of closely linked vertices $V = (v_1, v_2, \ldots, v_n)$ by counting the number of connections N_l with length l that part from one of the vertices of V. This local Rent exponent is a more detailed measure of the design's interconnection complexity.

s1488.bench

pins		gates		nets		vertices	
inputs	8	ANDs	350	1-point	19	fanout 2	109
outputs	19	ORs	200	2-point	573	fanout 3	400
		D-flipflops	6	3-point	22	fanout 4	116
		inverters	103	4 $\rightarrow$ 56-point	53	fanout 5	34
			659		667		659

Table 1: Information on benchmark "s1488.bench".

Note that with the definition of a local Rent exponent, the *global Rent exponent*, which is the one defined by Rent's rule, is computed by taking the sum of all interconnection length distributions over all the vertices. This sum will generally be dominated by the part with the highest (local) Rent exponent. This exponent will only equal the one defined in [LR71] if the design has a uniform interconnection complexity. Since the global Rent exponent only has a meaning in this case, our definition of a local Rent exponent matches the one for the global Rent exponent.

5 Results

In order to obtain some quantitative results, we placed some benchmark designs, using the technique of simulated annealing. In this section, the results obtained by a placement of the ISCAS89 benchmark designs "s1488.bench" and "s1494.bench" are presented. In tables 1 and 2, some information is given on these benchmarks.

The simulated annealing resulted for both designs in a nearly circular placement

s1494.bench

pins		gates		nets		vertices	
inputs	8	ANDs	354	1-point	19	fanout 2	95
outputs	19	ORs	204	2-point	567	fanout 3	405
		D-flipflops	6	3-point	22	fanout 4	118
		inverters	89	$4 \rightarrow 57$-point	53	fanout 5	35
			653		661		653

Table 2: Information on benchmark "s1494.bench".

of the vertices. The resulting interconnection length distributions are shown in the log-log diagrams of figures 6 and 7. In these diagrams, we fitted a line to the first 15 points using linear regression. We did not use the remaining data for higher lengths, because they depend too much on small changes in the placement. The Rent exponent of the design "s1488.bench" equals 0.71, while that of the design "s1494.bench" is 0.74. So, both designs have an almost equal interconnection complexity.

In both diagrams we see that the plotted points almost lie on a straight line. This means there is not a lot of variation over hierarchical levels. However, when we divide the design into four parts (associated with the four quadrants of the circle, obtained by the simulated annealing), we see that there are some minor local differences. The interconnection length distribution of the four parts is shown in figure 8 and 9 for "s1488.bench" and "s1494.bench" respectively.

The differences between the four parts in both benchmarks show that it makes sense to define a local Rent exponent. By using the interconnection length distribution we can compute the Rent exponent seperately for the parts.

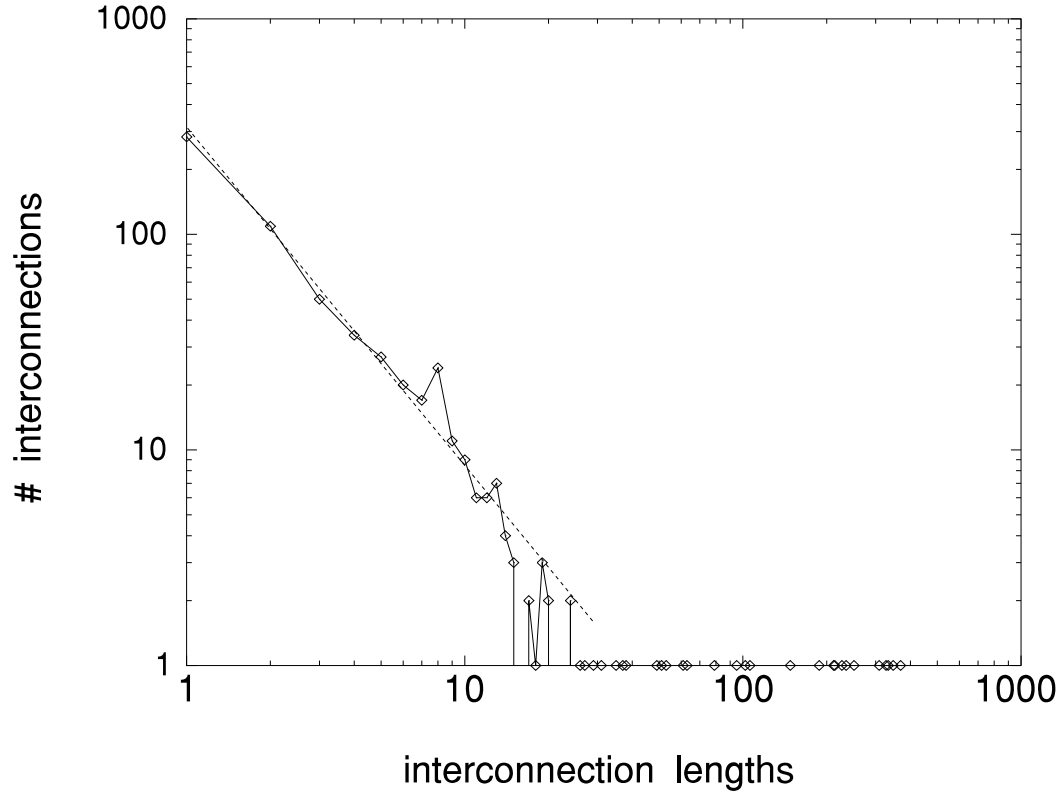

Figure 6: Interconnection length distribution for benchmark "s1488.bench" with best fitted line.

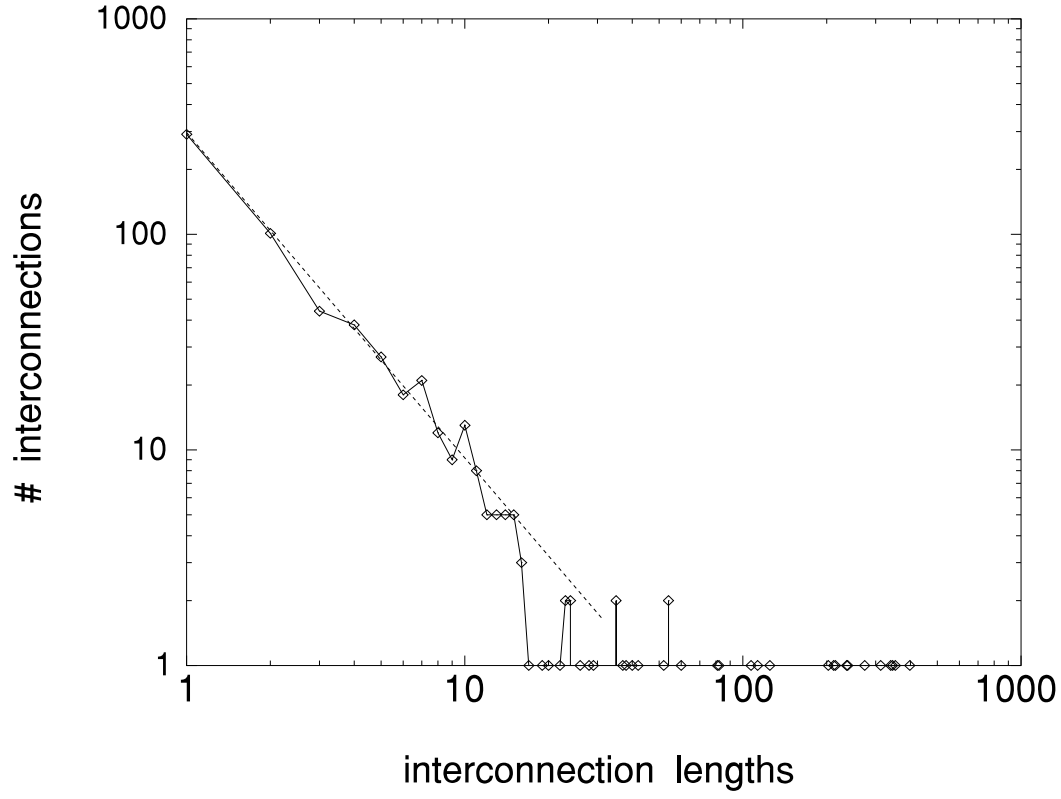

Figure 7: Interconnection length distribution for benchmark "s1494.bench" with best fitted line.

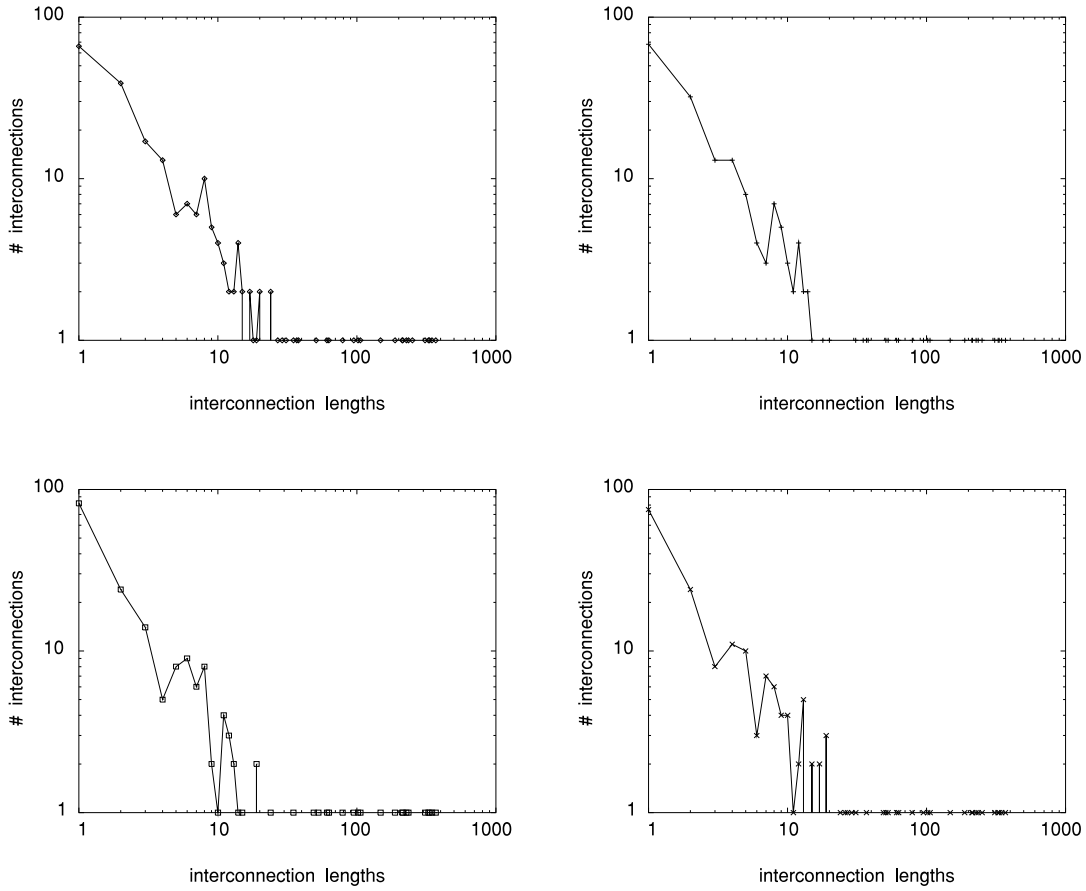

Figure 8: Interconnection length distribution for four parts of benchmark "s1488.bench".

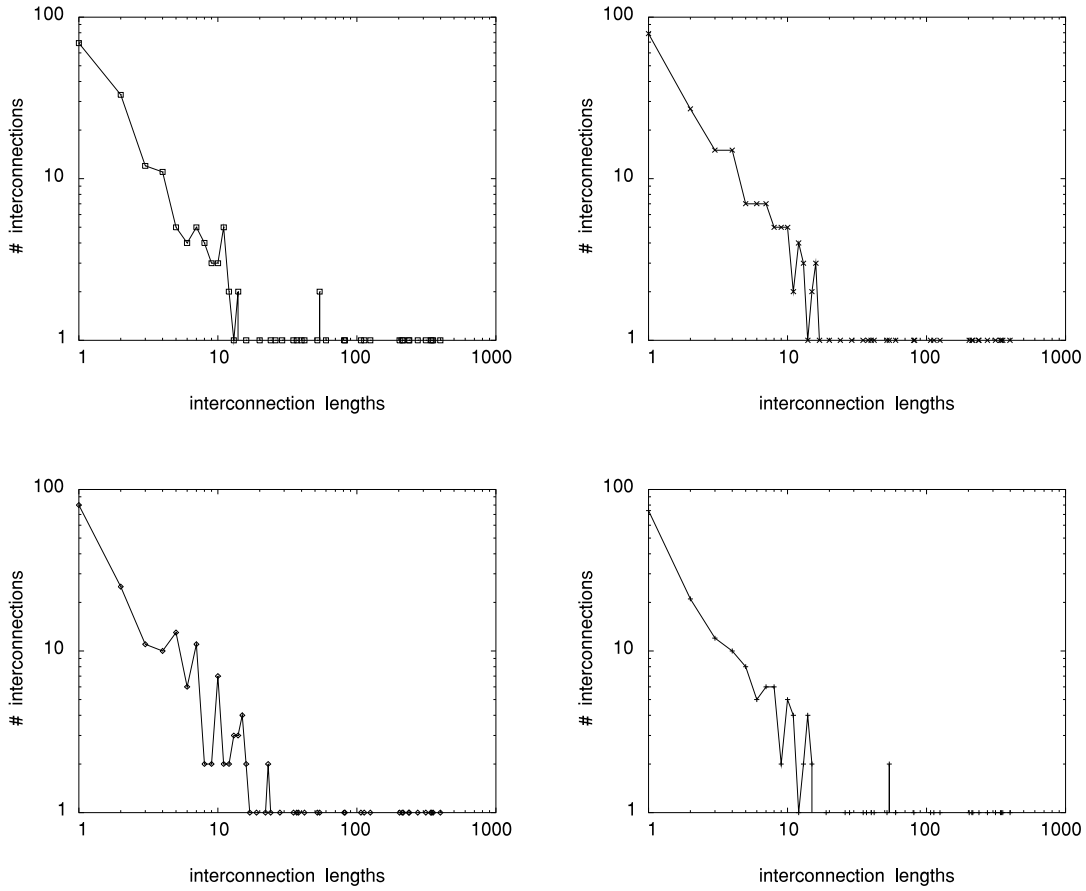

Figure 9: Interconnection length distribution for four parts of benchmark "s1494.bench".

6 Conclusion

In this paper, we showed that the Rent exponent r is not an accurate measure of the interconnection complexity when this complexity is not uniform over the design. An extension of Rent's rule is given to deal with locality in both hierarchy and space. For the latter, a new computation method for the Rent exponent r is presented, resulting in the definition of a local Rent exponent. With this new measure of interconnection complexity, a clear distinction can be made between more complex and less complex parts of the design, leading to more accurate estimations of layout properties.

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